

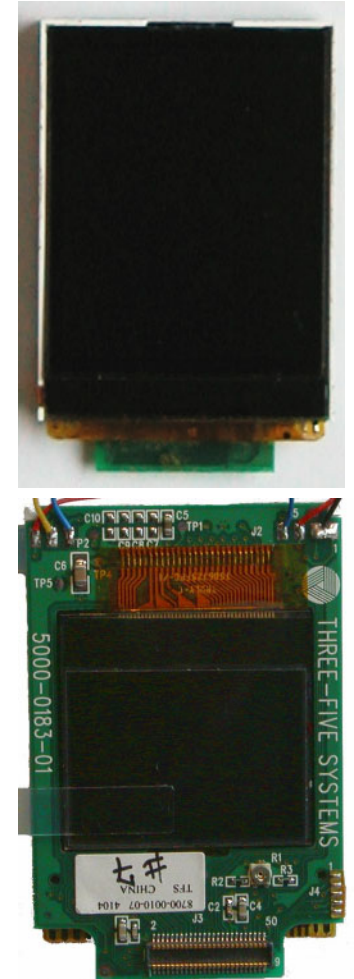


Display and backlight presentation

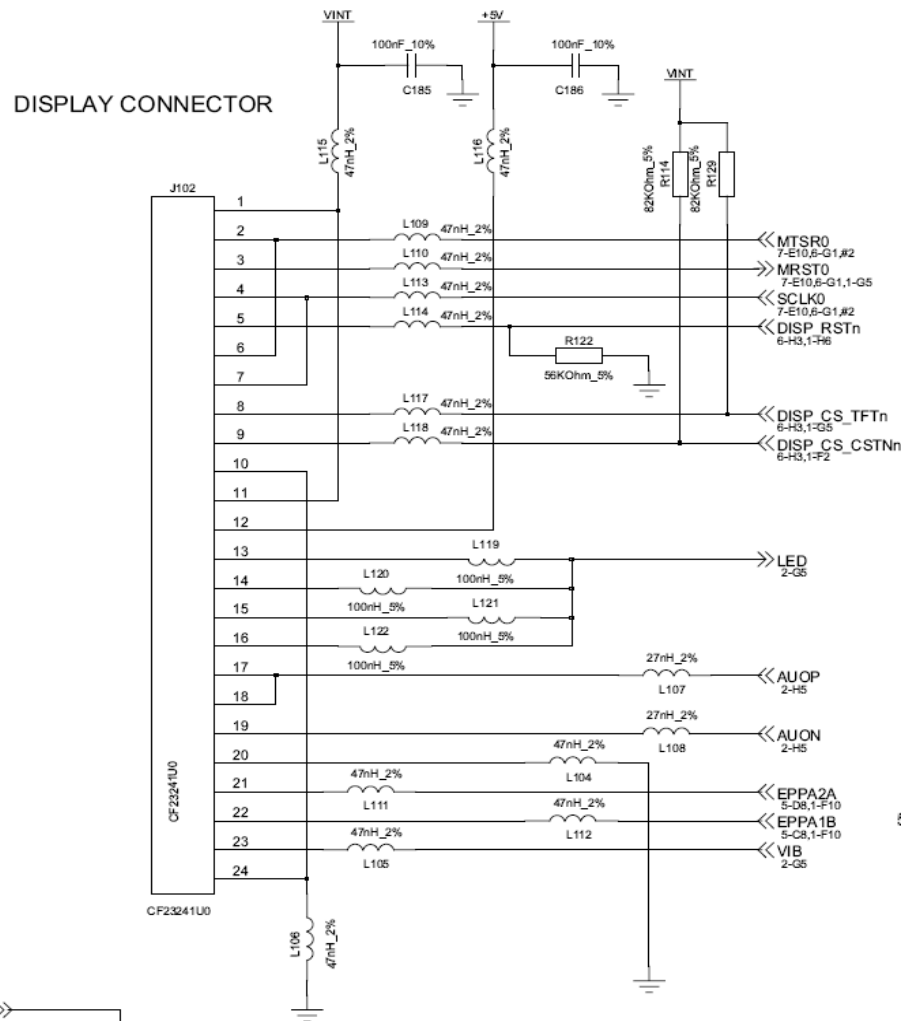
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Type of display used on globe 6

- 128RGBx160 COLOR 1.8" TFT LCD MODULE WITH 96xRGBx64 0.95" CSTN SECONDARY DISPLAY
- TFT use HD66337
- CSTN use SSD1788
- display is customized



Display interface – Globe 6 signals



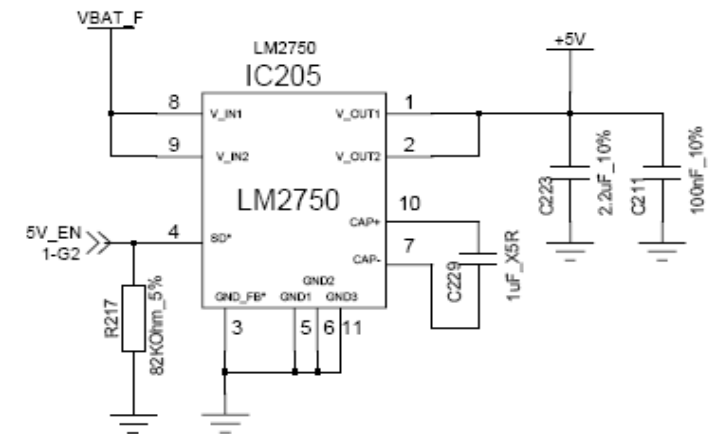
In our board both display are controlled with SPI signals.

Possibility to control the display through parallel line 18/16/9/8-bit for TFT and 8-bit for CSTN.

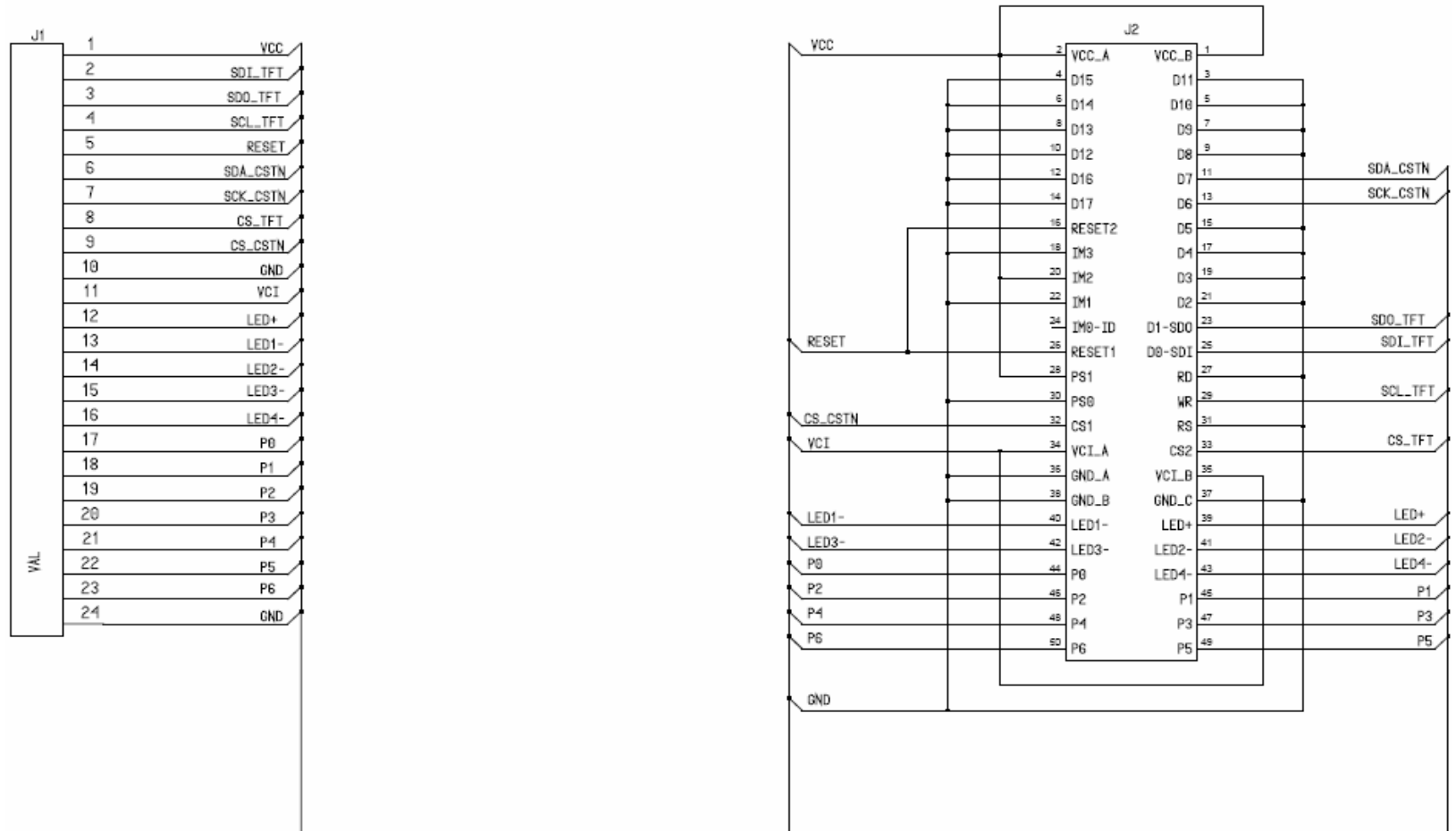
We have two CS to select the display.

Through the display path are take audio signal to the reviver and speaker and vibro.

Backlight is connected to +5V and controlled with LED signal from EPOWERLite.



Display interface - flex cable





Main display interface

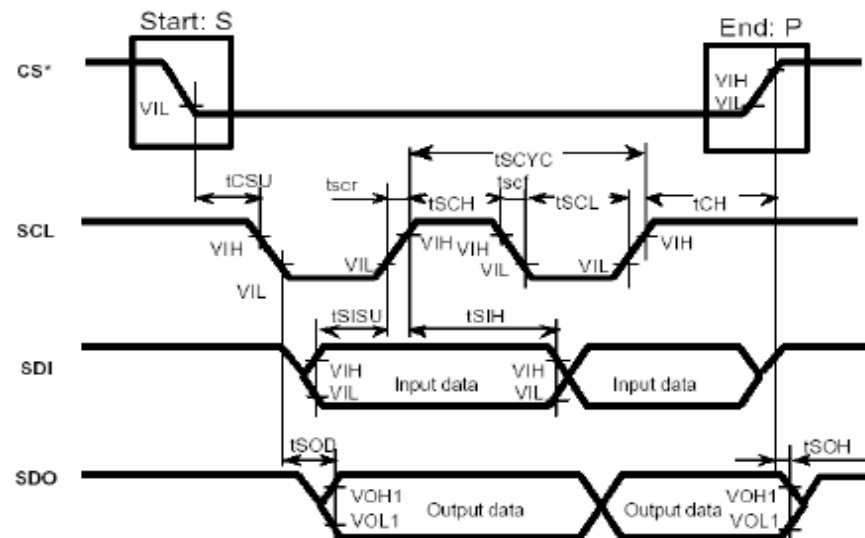
we have the possibility to send data and read data from TFT display

we can only send data to CSTN display

Main display interface

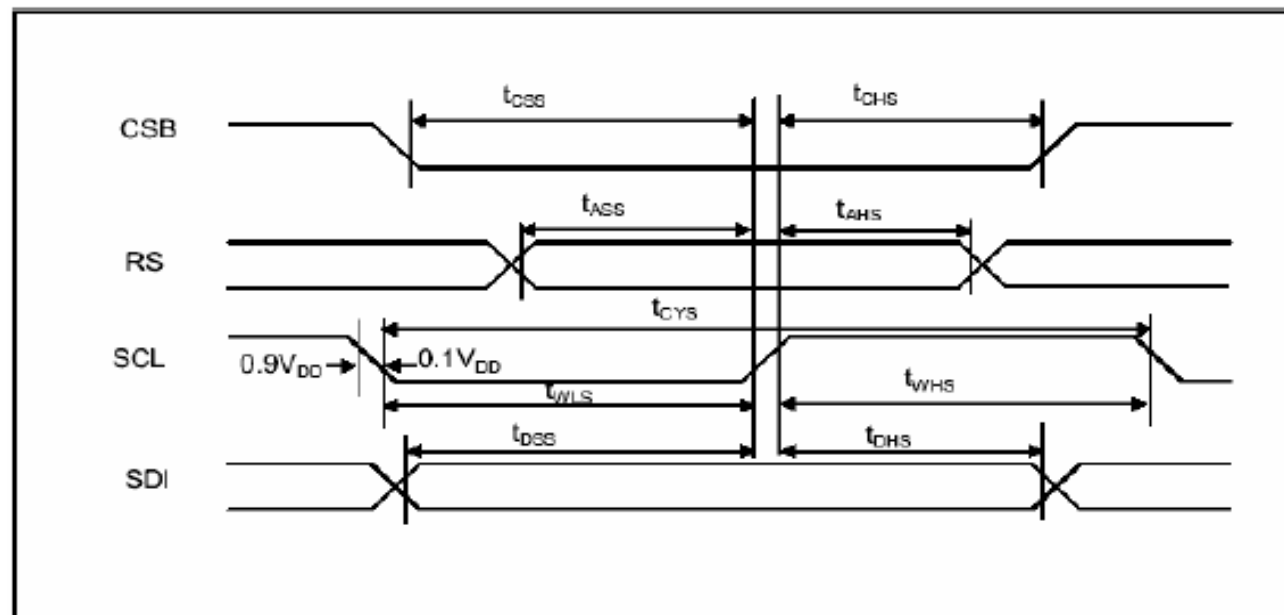
A.) Clock synchronized serial interface timing characteristics (VCC= 1.8V to 3.3V) - TFT

| Item | | Symbol | Unit | Min | Typ | Max |
|---------------------------------------|-------|------------|---------------|------|-----|-----|
| Serial clock cycle time | Write | tSCYC | μs | 0.1 | - | 20 |
| | Read | | | 0.35 | - | 20 |
| Serial clock 'high' level pulse width | Write | tSCH | ns | 40 | - | - |
| | Read | | | 150 | - | - |
| Serial clock 'low' level pulse width | Write | tSCL | ns | 40 | - | - |
| | Read | | | 150 | - | - |
| Serial clock rise/fall time | | tscr, tscf | ns | - | - | 20 |
| Chip select set up time | | tCSU | ns | 20 | - | - |
| Chip select hold time | | tCH | ns | 60 | - | - |
| Serial input data set up time | | tSISU | ns | 30 | - | - |
| Serial input data hold time | | tSIH | ns | 30 | - | - |
| Serial output data delay time | | tSOD | ns | - | - | 130 |
| Serial output data hold time | | tSOH | ns | 5 | - | - |



Second display interface

B.) Clock synchronized serial interface timing characteristics - CSTN



Write mode: $VCC = 2.4V$ to $3.3V$; $VCI = 2.6V$ (4) to $3.3V$; $VSS = 0V$; $T_{amb} = -20$ to $+50^{\circ}C$; unless otherwise specified.

| Item | Signal | Symbol | Min. | Typ. | Max. | Unit | Remark |
|-----------------------|--------|-----------|------|------|------|------|--------|
| Serial clock cycle | SCL | t_{CYS} | 250 | - | - | ns | |
| SCLK high pulse width | | t_{WHS} | 100 | - | - | | |
| SCLK low pulse width | | t_{WLS} | 100 | - | - | | |
| Address setup time | RS | t_{ASS} | 150 | - | - | ns | |
| Address hold time | | t_{AHS} | 150 | - | - | | |
| Data setup time | SDI | t_{DSS} | 100 | - | - | ns | |
| Data hold time | | t_{DHS} | 100 | - | - | | |
| CSB setup time | CSB | t_{CSS} | 150 | - | - | ns | |
| CSB hold time | | t_{CHS} | 150 | - | - | | |

Second display interface

– DC electrical characteristics

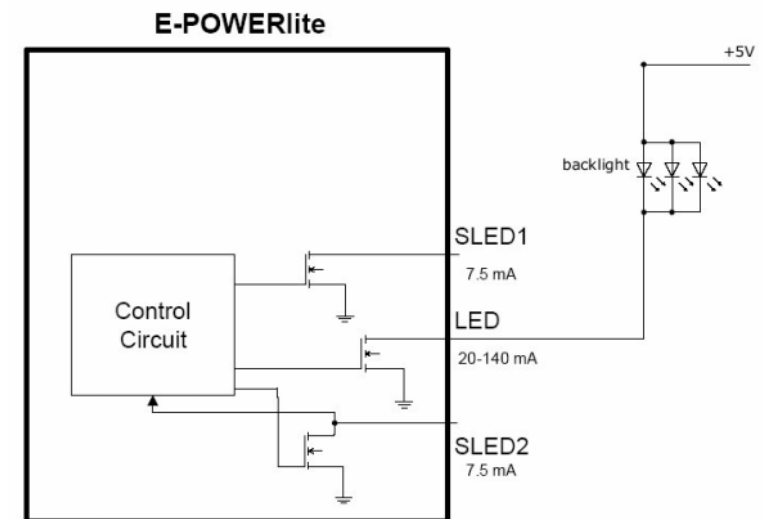
| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---|--------|-------------|--------|-----|---------|------|
| Power supply voltage (logic) | VCC | - | 1.80 | 2.8 | 3.30 | V |
| Power supply voltage (analog) | VCI | - | 2.60 | 2.8 | 3.30 | V |
| Input voltage (logic) (note 1) | Vi | 'H' level | 0.8VCC | - | VDD | V |
| | | 'L' level | 0 | - | 0.15VCC | |
| Power supply current consumption (note 2, 3, 4, 5, 6) | ICC | All white | - | TBD | - | μA |
| | | B&W checker | - | TBD | - | |
| | | Partial | - | TBD | - | |
| | | Sleep | - | TBD | - | |
| | | Standby | - | TBD | - | |
| Power supply current consumption (note 2, 3, 4, 5, 6) | ICI | All white | - | TBD | - | μA |
| | | B&W checker | - | TBD | - | |
| | | Partial | - | TBD | - | |
| | | Sleep | - | TBD | - | |
| | | Standby | - | TBD | - | |
| Frame frequency (TFT) | fFLM | - | - | 88 | - | Hz |
| Frame frequency (CSTN) | fFLM | - | 35 | 70 | 95 | Hz |

Note: Items marked with an asterisk (*) are design targets.

Displays backlight

■ Both display

- display backlight is directly controlled from EPOWERlite
 - programable from 20mA to 140mA with setps of 20mA
 - duty cycle of LED current can be set from 0.5% to 100% in 63 steps





Display and backlight presentation

End of story.

Thanks