Service Repair Documentation
Level 2.5e – SL65

Release	Date	Department	Notes to change
1.0	13.08.2004	ICM MP CCQ GRM T	New document

Table of Contents:

1 List of available level 2,5e parts SL65

Component Typ/Circuit Part	Component Details	ID	Partnumber
ASIC	Power Supply D1094DA MOZART_TWIGO4	D1300	L36145-J4683-Y19
ASIC	Camera_Interface S1D13716B02	D3601	L36820-U6054-D670
Cap_Diode_26MHz_Circuit	Cap_Diode_1SV305	V3961	L36840-D61-D670
Capacitor_Mozart_Twigo_Circuit	Capacitor 2*2U2	C1329	L36344-F1225-M12
Capacitor_Mozart_Twigo_Circuit	Capacitor 2*2U2	C1330	L36344-F1225-M12
Capacitor_Mozart_Twigo_Circuit	Capacitor 2*2U2	C1332	L36344-F1225-M12
Coil_BATT+	Coil 500 OHM	L1300	L36140-F100-Y10
Coil_VBOOST	Coil 4U7	L1302	L36151-F5472-M2
Coil_VBOOST	Coil HM331	L1303	L36140-F1100-Y5
Coil_VBUCK	Coil 10U	L1301	L36151-F5103-M
Diode_VBOOST	Diode BAT760	V1303	L36840-D5076-D670
Diode_VBUCK	Diode BAT760	V1302	L36840-D5076-D670
Filter_IO Interface	EMI_EMV_Filter_IP4559CX25	Z1500	L36820-L6147-D670
IC MODUL PA	PF08143B SMD	N3981	L36851-Z2002-A77
IC_FEM	FEM TDK GSM900 1800 1900	N3901	L36145-K280-Y258
IC_Processor_SGOLDLITE	PMB8875 V1X	D1000	L36810-G6191-D670
IC_Transceiver	HD155155NPEB	N3921	L36820-L6142-D670
Oszillator_RF_Logic	Oszillator_26MHz	Z3961	L36145-F260-Y17
Oszillator_RTC	Oszillator_32,768KHZ	Z1000	L36145-F102-Y22
Resistor_Temp_TVCXO	Resistor_Temp 22k R	R3967	L36120-F4223-H
Switch_USB	NC7WB66K8X DUAL BUS SWITCH	N1501	L36810-B6132-D670
Trans_Charge_Circuit	Transistor SI5933DC	V1305	L36830-C1107-D670
Trans_DISPLAY_BACKLIGHT	Transistor EMB9/PEMB9	V2303	L36840-C4059-D670
Trans_V2.65V	Transistor EMD12	V1500	L36840-C4057-D670
Trans_VBOOST	Transistor FDG313N	V1304	L36830-C1121-D670
Volt.Regulator_Camera	Volt.Reg. LP1986_2*2.85V	N3600	L36810-C6065-D670
Filter_SIM Interface	EMI_Filter SIM PROTECTION	Z1605	L36820-U6056-D670
Trans_DISPLAY_BACKLIGHT	Transistor BCS 46S	V2302	L36840-C4014-D670
Trans_DISPLAY_BACKLIGHT	Transistor BCS 46S	V2304	L36840-C4014-D670
Trans_DISPLAY_BACKLIGHT	Transistor BCS 46S	V2821	L36840-C4014-D670
Filter_Side Key Interface	EMI_Filter Side Key Protection	Z2900	L36820-U6065-D670
Switch	LOW POWER HALL SWITCH	S3251	L36197-F5008-F63
Switch	LOW POWER HALL SWITCH	S3252	L36197-F5008-F63

2 Required Equipment for Level 2,5e

- GSM-Tester (CMU200 or 4400S incl. Options)
- PC-incl. Monitor, Keyboard and Mouse
- Bootadapter 2000/2002 (L36880-N9241-A200)
- Adapter cable for Bootadapter due to ***new*** Lumberg connector (F30032-P226-A1)
- Troubleshooting Frame SL65 (F30032-P419-A1)
- Power Supply (at least one GRT required power supply)
- Spectrum Analyser
- Active RF-Probe incl. Power Supply
- Oscilloscope incl. Probe
- RF-Connector (N<>SMA(f))
- Power Supply Cables
- Dongle (F30032-P28-A1) if USB-Dongle is used a special driver for NT is required
- BGA Soldering equipment

Reference: Equipment recommendation Version X (newest version)
(downloadable from the technical support page)

3 Required Software for Level 2,5e SL65

- Winsui for 65series
- Software for GSM-Tester (GRT)
- Software for reference oscillator adjustment
- Internet unblocking solution (JPICS)
- Dongle driver for dongle protected Siemens software tools

4 Radio Part

The radio part realizes the conversion of the GMSK-HF-signals from the antenna to the base-band and vice versa.

In the receiving direction, the signals are split in the I- and Q-component and led to the D/A-converter of the logic part. In the transmission direction, the GMSK-signal is generated in an Up Conversion Modulation Phase Locked Loop by modulation of the I- and Q-signals which were generated in the logic part. After that the signals are amplified in the power amplifier.

Transmitter and Receiver are never active at the same time. Simultaneous receiving in two bands is impossible. Simultaneous transmission in two bands is impossible, too. However the monitoring band (monitoring timeslot) in the TDMA-frame can be chosen independently of the receiving respectively the transmitting band (RX- and TX timeslot of the band).

The RF-part of the SL65 are dimensioned for triple band operation (EGSM900, GSM1800, GSM1900) supporting GPRS functionality up to multiclass 10.

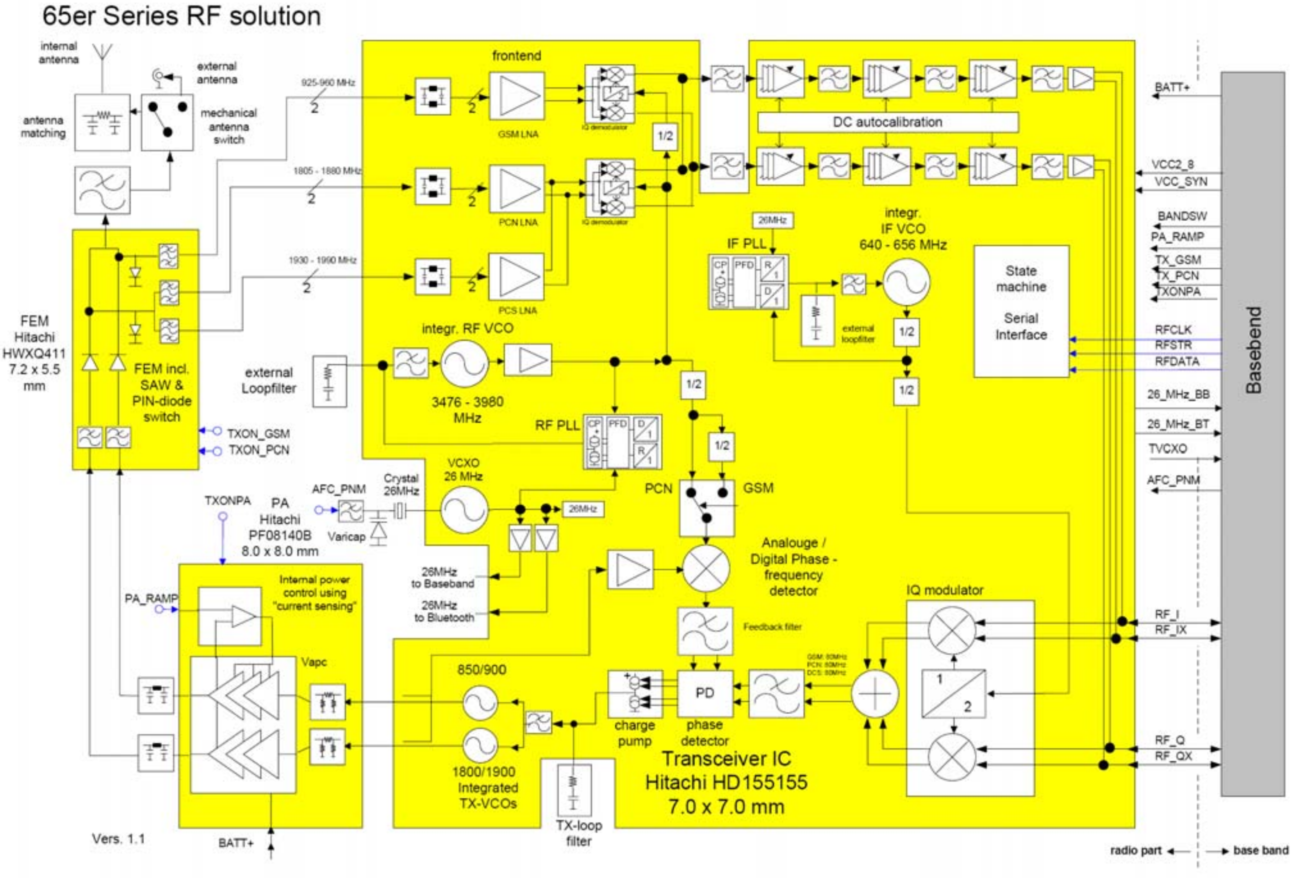
The RF-circuit consists of the following components:

- Hitachi Bright VE chip set with the following functionality:
  - PLL for local oscillator LO1 and LO2 and TxVCO
  - Integrated local oscillators LO1, LO2 (without loop filter)
  - Integrated TxVCO (without loop filter and core inductors for GSM)
  - Direct conversion receiver including LNA, DC-mixer, channel filtering and PGC-amplifier
  - Active part of 26 MHz reference oscillator
- Hitachi LTCC transmitter power amplifier with integrated power control circuitry
- Hitachi Frontend-Module including RX-/TX-switch and EGSM900 / GSM1800 / GSM 1900 receiver SAW-filters

Quartz and passive circuitry of the 26MHz VCXO reference oscillator.

SIEMENS mobile

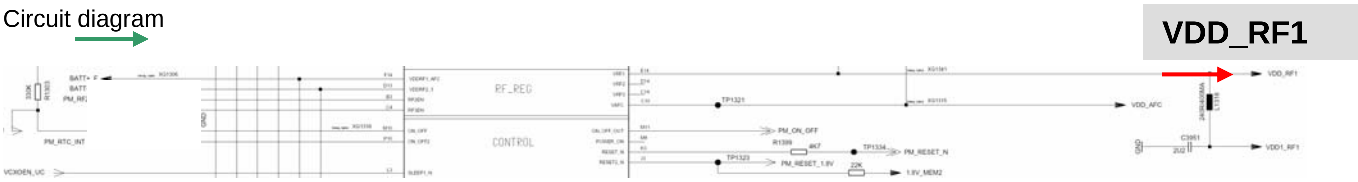
4.1 Block diagram RF part



4.2 Power Supply RF-Part

The voltage regulator for the RF-part is located inside the ASIC D1300. (see chapter 5.2).It generates the required 2,85V "RF-Voltage" named VDD_RF1(VDD_BRIGHT). The voltage regulator is activated as well as deactivated via VCXOEN_UC (Functional F23) provided by the SGOLDLITE+. The temporary deactivation is used to extend the stand by time.

Circuit diagram



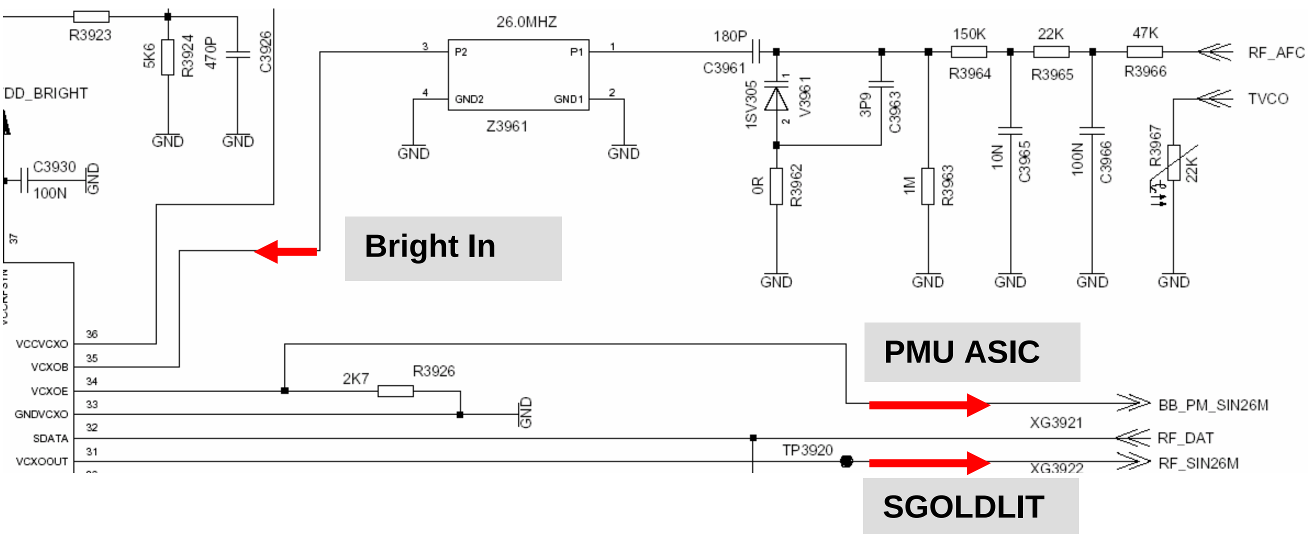
4.3 Frequency generation

4.3.1 Synthesizer: The discrete VCXO (26MHz)

The SL65 mobile is using a reference frequency of 26MHz. The generation of the 26MHz signal is done via a TXVCO. This oscillator consists mainly of the 26MHz TXVCO, Z3961 and the capacity diode, V3961.

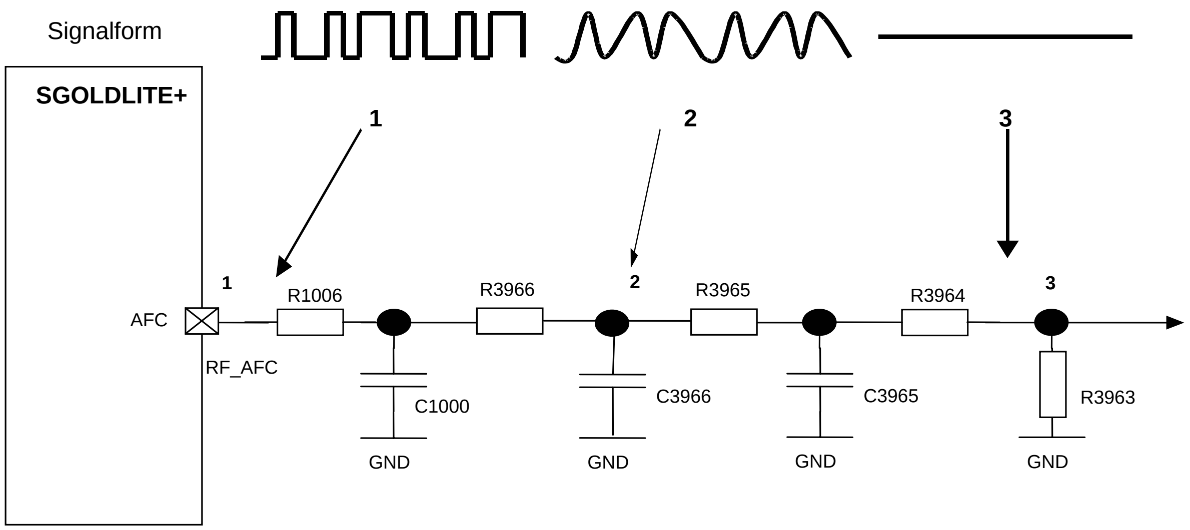
TP (test point) of the 26MHz signal is the TP 3920

The oscillator output signal 26MHz_RF is directly connected to the BRIGHT IC (pin 35) to be used as reference frequency inside the Bright (PLL). The signal leaves the Bright IC as RF_SIN26M (pin 31) to be further used from the SGOLDLITE+ (D171 **(Functional AE15)**) and as BB_PM_SIN26M (pin 34) as clock for the DA converter inside the PMU ASIC.



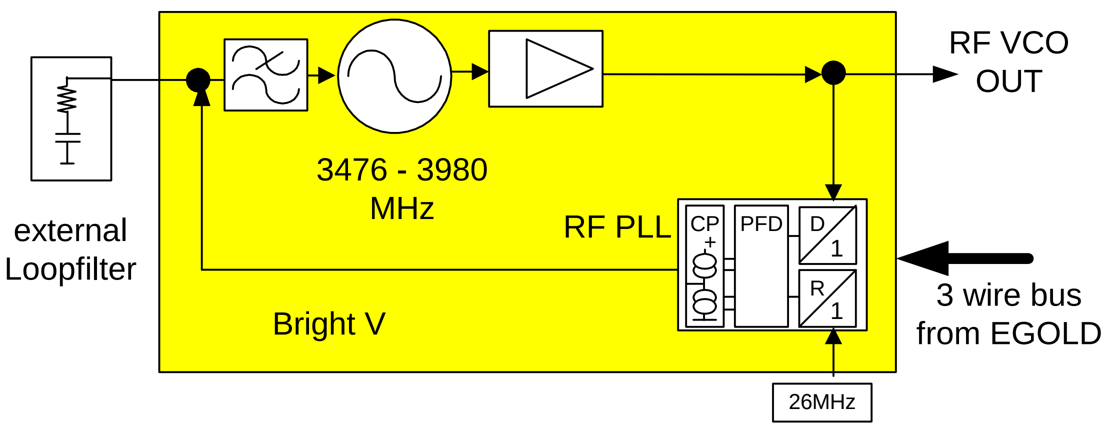
To compensate frequency drifts (e.g. caused by temperature) the oscillator frequency is controlled by a (RF_AFC) signal, generated through the internal SGOLDLITE (D1000 (Functional A9)) PLL via the capacity diode V3961. For temperature measurements of the VCXO a temperature-dependent resistance is used. Reference for the "SGOLDLITE-PLL" is the base station frequency received via the Frequency Correction Burst.

Waveform of the AFC_PNM signal from SGOLDLITE+ to Oscillator



4.3.2 Synthesizer: RFVCO(LO1)

The first local oscillator (LO1) consists of a PLL and VCO inside Bright (N3921) and an external loop filter The first local oscillator is needed to generate frequencies which enable the transceiver IC to demodulate the receiver signal and to perform the channel selection in the TX part. To do so, a control voltage for the LO1 is used, gained by a comparator. This control voltage is a result of the comparison of the divided LO1 and the 26MHz reference Signal. The division ratio of the dividers is programmed by the SGOLDLITE+, according to the network channel requirements.

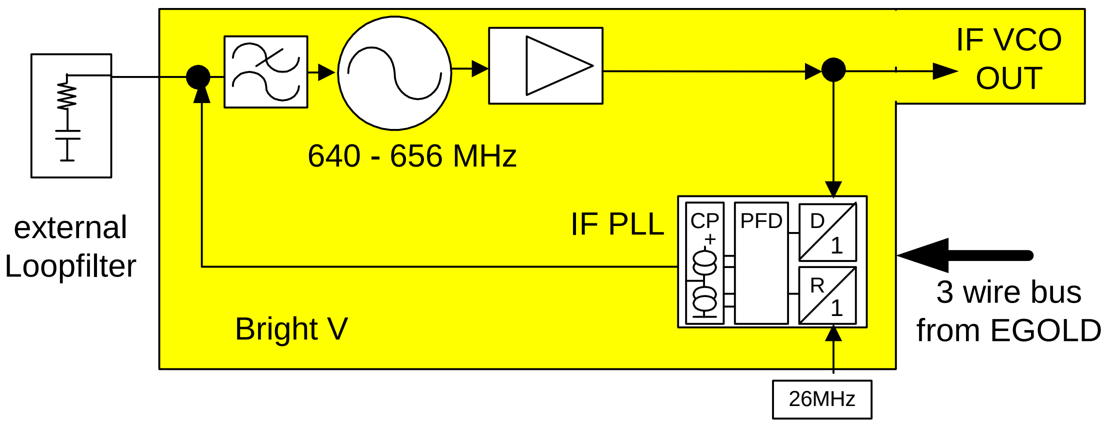


Matrix to calculate the TX and RX frequencies

Band	RX / TX	Channels	RF frequencies	LO1 frequency	IF freq.
EGSM 900	Receive:	0..124	935,0 - 959,8 MHz	LO1 = 4*RF	
EGSM 900	Transmit:	0..124	890,0 - 914,8 MHz	LO1 = 4*(RF+IF)	80,0 MHz
EGSM 900	Receive:	975..1023	925,2 - 934,8 MHz	LO1 = 4*RF	
EGSM 900	Transmit:	975..1023	880,2 - 889,8 MHz	LO1 = 4*(RF+IF)	82,0 MHz
GSM 1800	Receive:	512..661	1805,2 - 1835,0 MHz	LO1 = 2*RF	
GSM 1800	Transmit:	512..661	1710,2 - 1740,0 MHz	LO1 = 2*(RF+IF)	80,0 MHz
GSM 1800	Receive:	661..885	1835,0 - 1879,8 MHz	LO1 = 2*RF	
GSM 1800	Transmit:	661..885	1740,0 - 1784,8 MHz	LO1 = 2*(RF+IF)	82,0 MHz

4.3.3 Synthesizer: IFVCO(LO2)

The second local oscillator (LO2) consists of a PLL and a VCO which are integrated in Bright and a second order loopfilter which is realized external (R3927; C3940; C3948). Due to the direct conversion receiver architecture, the LO2 is only used for transmit-operation. The LO2 covers a frequency range of at least 16 MHz (640MHz – 656MHz).
Before the LO2-signal gets to the modulator it is divided by 8. So the resulting TX-IF frequencies are 80/82 MHz (dependent on the channel and band). The LO2 PLL and power-up of the VCO is controlled via the tree-wire-bus of Bright (SGOLDLITE+ signals RFDATA; RFCLK; RFSTR). To ensure the frequency stability, the 640MHz VCO signal is compared by the phase detector of the 2^{nd} PLL with the 26Mhz reference signal. The resulting control signal passes the external loop filter and is used to control the 640/656MHz VCO.



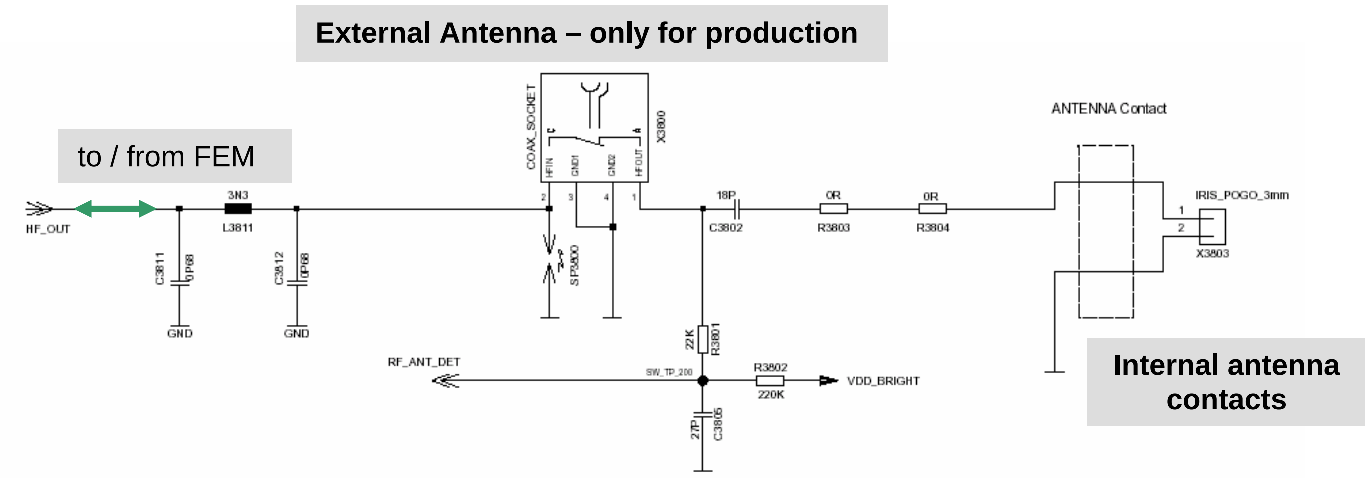
4.3.4 Synthesizer: PLL

The frequency-step is 400 kHz in GSM1800/GSM1900 mode and 800kHz in EGSM900 mode due to the internal divider by two for GSM1800/GSM19000 and divider by four for EGSM900. To achieve the required settling-time in GPRS operation, the PLL can operate in fastlock-mode a certain period after programming to ensure a fast settling. After this the loopfilter and currents are switched into normal-mode to get the necessary phasenoise-performance. The PLL is controlled via the tree-wire-bus of Bright.

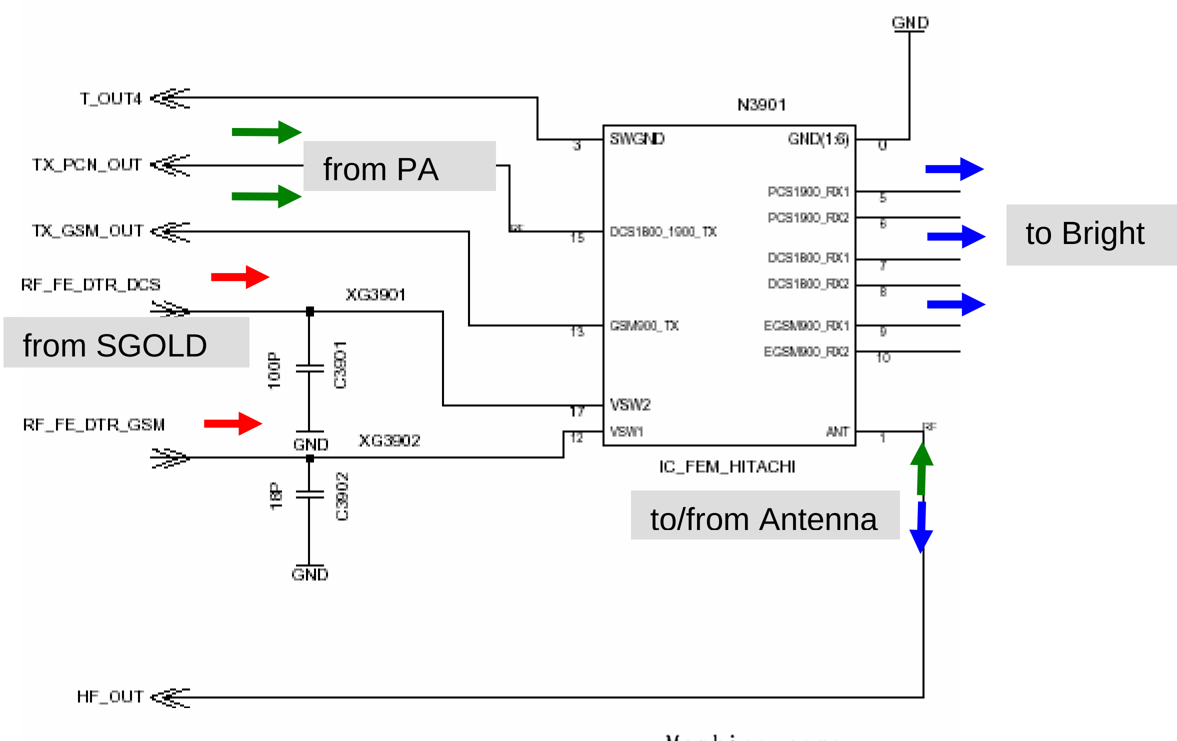
4.4 Antenna switch (electrical/mechanical)

Internal/External <> Receiver/Transmitter
The mobile have two antenna switches.

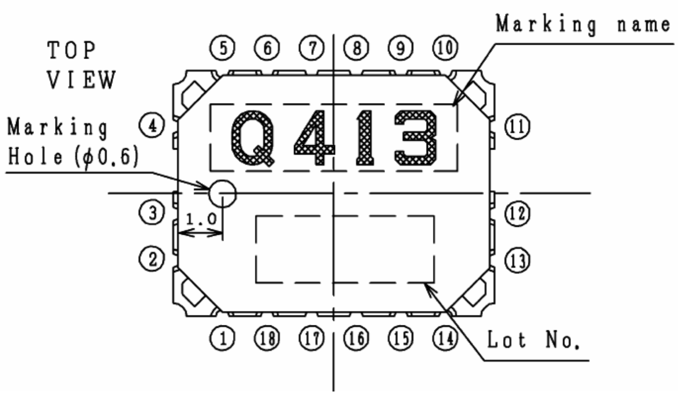
a) The mechanical antenna switch for the differentiation between the internal and external antenna, which is used only production.



b) The electrical antenna switch, for the differentiation between the receiving and transmitting signals. To activate the correct settings of this diplexer, the SGOLDLITE signals RF_FE_DTR_DCS (to activate TX GSM1800 and GSM1900) and RF_FE_DTR_GSM (to activate TX GSM900) are required.



Top View



Switching Matrix

Select Mode	Vc(EGSM)	Vc(DCS/PCS)
EGSM-RX	Low	Low
EGSM-TX	High	Low
DCS -RX	Low	Low
PCS-RX	Low	Low
DCS/PCS-TX	Low	High

Pin assignment

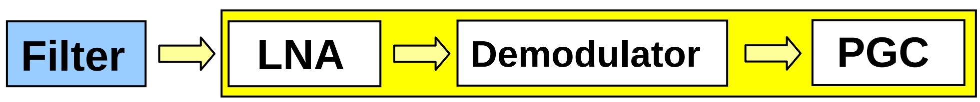
Pin. No	Function
①	ANT
⑤	PCS Rx-1
⑥	PCS Rx-2
⑦	DCS Rx-1
⑧	DCS Rx-2
⑨	EGSM Rx-1
⑩	EGSM Rx-2
⑫	EGSM-CONT.
⑬	EGSM-Tx
⑮	DCS/PCS-Tx
⑰	DCS/PCS-CONT.
②③④ ⑪⑭⑯ ⑱	GND

4.5 Receiver

Receiver: Filter to Demodulator

The band filters are located inside the frontend module (N3901). The filters are centred to the band frequencies. The symmetrical filter output is matched to the LNA input of the Bright (N3921).The Bright VE incorporates three RF LNAs for GSM850/EGSM900, GSM1800 and GSM1900 operation. The LNA/mixer can be switched in High- and Low-mode to perform an amplification of ~ 20dB. For the “High Gain“ state the mixers are optimised to conversion gain and noise figure, in the “Low Gain“ state the mixers are optimised to large-signal behaviour for operation at a high input level. The Bright performs a direct conversion mixers which are IQ-demodulators. For the demodulation of the received GSM signals the LO1 is required. The channel depending LO1 frequencies for 1800MHz/1900MHz bands are divided by 2 and by 4 for 850MHG/900MHz band. Furthermore the IC includes a programmable gain baseband amplifier PGA (90 dB range, 2dB steps) with automatic DC-offset calibration. LNA and PGA are controlled via SGOLDLITE signals RFDATA; RFCLK; RFSTR(**RF_Ctrl C8, B10, B12**). The channel-filtering is realized inside the chip with a three stage baseband filter for both IQ chains. Only two capacitors which are part of the first passive RC-filters are external. The second and third filters are active filters and are fully integrated. The IQ receive signals are fed into the A/D converters in the EGAIM part of SGOLDLITE+. The post-switched logic measures the level of the demodulated baseband signal and regulates the level to a defined value by varying the PGA amplification and switching the appropriate LNA gains.

From the antenna switch, up to the demodulator the received signal passes the following blocks to get the demodulated baseband signals for the SGOLDLITE+:



N3901 **Bright(N3921)**

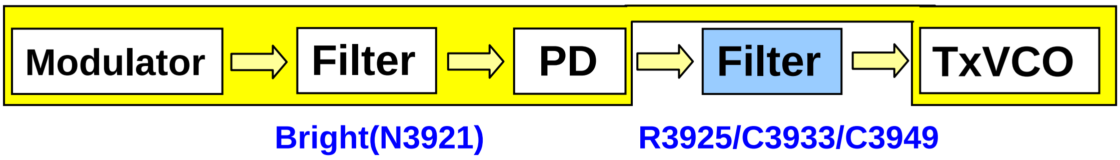
4.6 Transmitter

4.6.1 Transmitter: Modulator and Up-conversion Loop

Transmitter

Up conversion loop

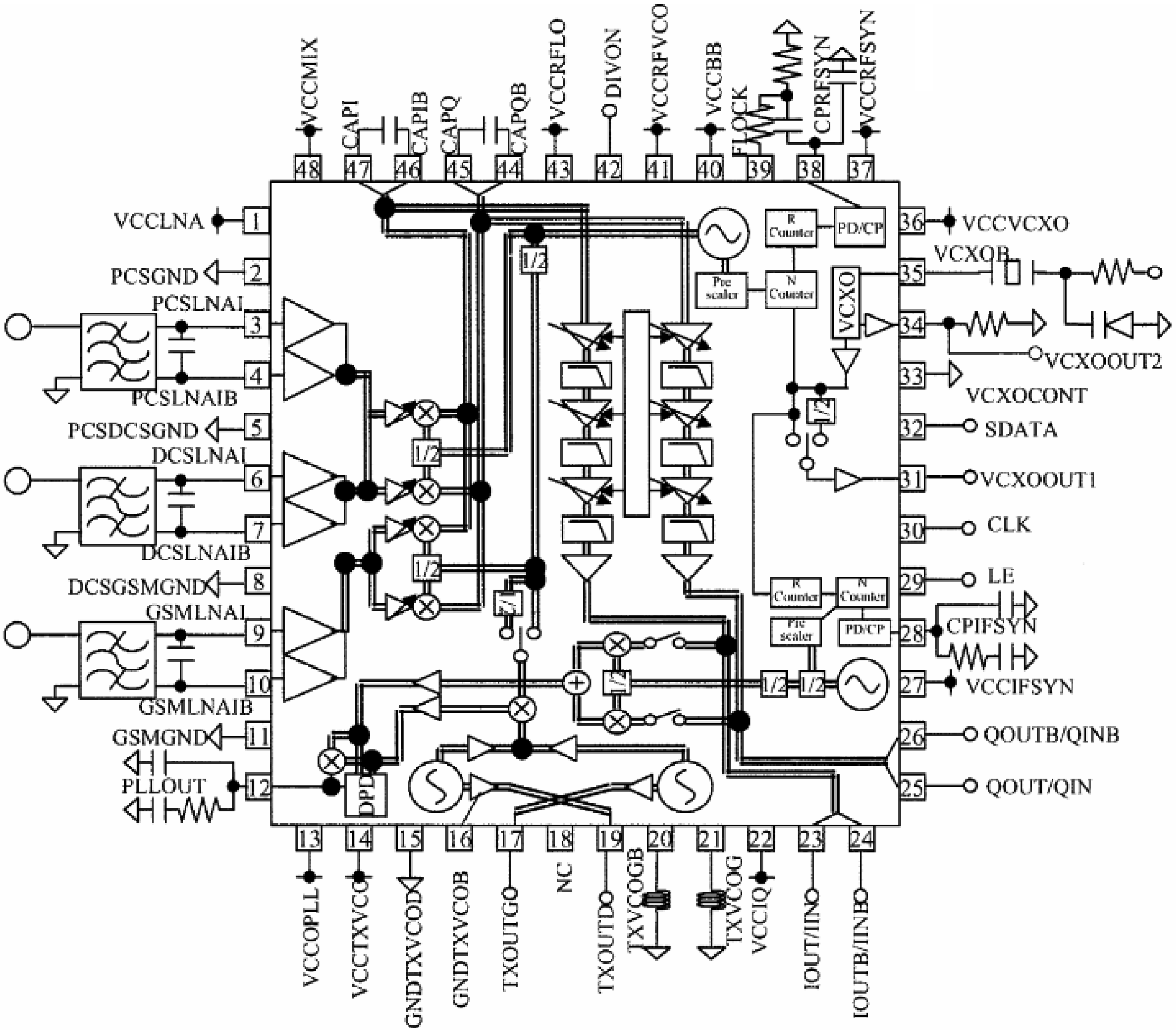
The generation of the GMSK-modulated signal in Bright (N3921) is based on the principle of up conversion modulation phase locked loop. The incoming IQ-signals from the baseband are mixed with the divided LO2-signal. The modulator is followed by a lowpass filter (corner frequency ~80 MHz) which is necessary to attenuate RF harmonics generated by the modulator. A similar filter is used in the feedback-path of the down conversion mixer.
With help of an offset PLL the IF-signal becomes the modulated signal at the final transmit frequency. Therefore the GMSK modulated rf-signal at the output of the TX-VCOs is mixed with the divided LO1-signal to a IF-signal and sent to the phase detector. The I/Q modulated signal with a centre frequency of the intermediate frequency is send to the phase detector as well.
The output signal of the phase detector controls the TxVCO and is processed by a loop filter whose components are external to the Bright. The TxVCO which is realized inside the Bright chip generates the GSMK modulated frequency.



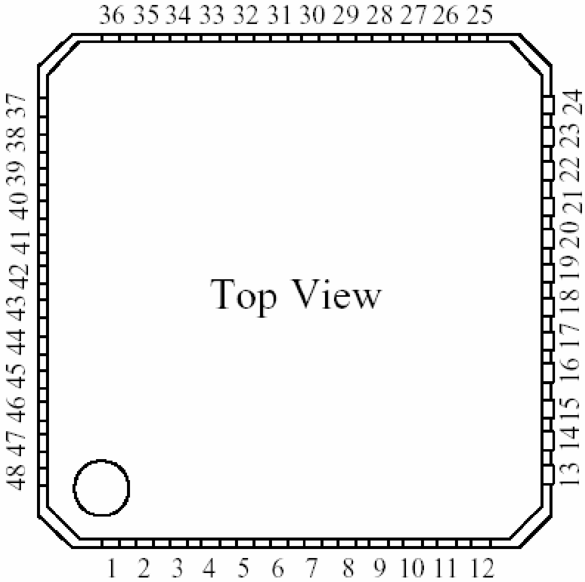
4.7 Bright IC Overview

BRIGHT VE

IC Overview



IC Top View



IC Pin assignment

Pin No	Pin Name	Description	Pin No	Pin Name	Description
1	VCCLNA	VCC for LNA transistor and LNA Bias	25	QOUT/QIN	Positive output/input of Q channel/modulator
2	PCSGND	GND for Emitter of LNA transistor(PCS)	26	QOUTB/QINB	Negative output/input of Q channel/modulator
3	PCSLNAI	Positive input for LNA transistor(PCS)	27	VCCIFSYN	VCC for IFVCO Buffer and Divider, and IF synthesiser
4	PCSLNAIB	Negative input for LNA transistor(PCS)	28	CPIFSYN	Charge Pump output of IF synthesiser
5	PCSDCSGND	GND for Emitter of LNA transistor(PCS,DCS)	29	LE	Load enable for serial data
6	DCSLNAI	Positive input for LNA transistor(DCS)	30	CLK	Clock for serial data
7	DCSLNAIB	Negative input for LNA transistor(DCS)	31	VCXOOUT1	Output for VCXO (for Base Band LSI)
8	DCSGSMGND	GND for Emitter of LNA transistor(DCS,GSM)	32	SDATA	Serial Data
9	GSMLNAI	Positive input for LNA transistor(GSM)	33	VCXOCONT	VCXO / TCXO control input
10	GSMLNAIB	Negative input for LNA transistor(GSM)	34	VCXOOUT2	Output for VCXO (open emitter of buffer transistor)
11	GSMGND	GND for Emitter of LNA transistor(GSM)	35	VCXOB	Base of VCXO transistor
12	PLLOUT	Current output to control and modulate TXVCO	36	VCCVCXO	VCC for VCXO
13	VCCOPLL	VCC for OPLL and Phase comparator	37	VCCRFSYN	VCC for RF synthesiser
14	VCCTXVCO	VCC for TXVCO	38	CPRFSYN	Charge Pump output of RF synthesiser
15	GNDTXVCOD	GND for DCS/PCS TxVCO	39	FLOCK	Fast Lock control for RF synthesiser
16	GNDTXVCOB	GND for TXVCO Output Buffer	40	VCCBB	VCC for Base band and State Logic
17	TXOUTG	Tx output for GSM	41	VCCRFVCO	VCC for RF VCO
18	NC	No Connect	42	DIVON	VCXOOUT divider control input
19	TXOUTD	Tx output for DCS/PCS	43	VCCRFLO	VCC for RF Local Buffer and Divider
20	TXVCOGB	Negative TxVCO output for GSM	44	CAPQB	Capacitor for Q channel LPF(Negative output)
21	TXVCOG	Positive TxVCO output for GSM	45	CAPQ	Capacitor for Q channel LPF(Positive output)
22	VCCIQ	VCC for IQ modulator	46	CAPIB	Capacitor for I channel LPF(Negative output)
23	IOUT/IIN	Positive output/input of I channel/modulator	47	CAPI	Capacitor for I channel LPF (Positive output)
24	IOUTB/IINB	Negative output/input of I channel/modulator	48	VCCMIX	VCC for Direct conversion Mixer

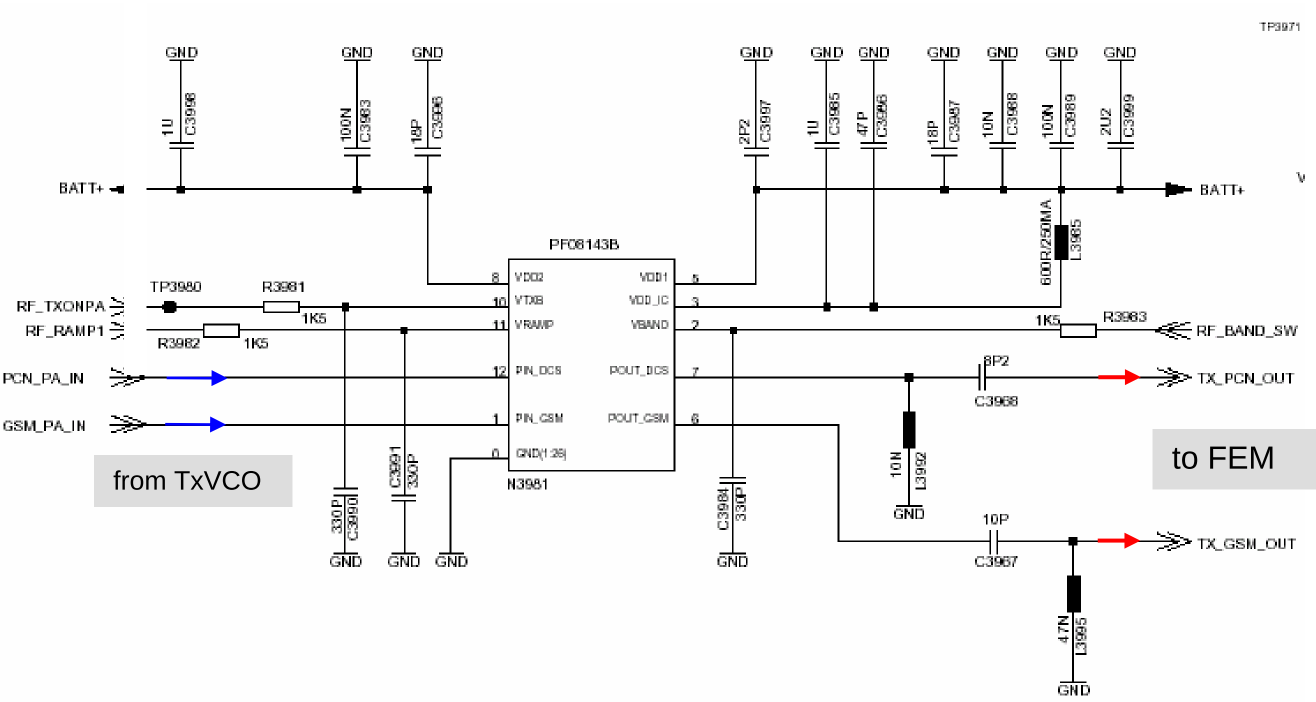
4.7.1 Transmitter: Power Amplifier

The output signals (PCN_PA_IN, and GSM_PA_IN) from the TxVCO are led to the power amplifier. The power amplifier is a PA-module N3981 from Hitachi. It contains two separate 3-stage amplifier chains EGSM900 and GSM1800 / GSM1900 operation. It is possible to control the output-power of both bands via one VAPC-port. The appropriate amplifier chain is activated by a logic signal RF_BAND_SW**(GSM TDMA-Timer A10)** which is provided by the SGOLDLITE+.

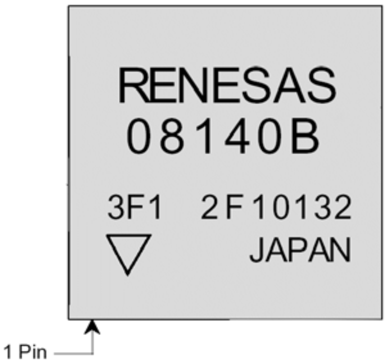
To ensure that the output power and burst-timing fulfills the GSM-specification, an internal power control circuitry is use. The power detect circuit consists of a sensing transistor which operates at the same current as the third rf-transitor. The current is a measure of the output power of the PA. This signal is square-root converted and converted into a voltage by means of a simple resistor. It is then compared with the RF_RAMP1**(Analog Interface J2)** signal. The N3981 is activated through the signal RF_TXONPA**(GSM TDMA-Timer A17)**.

The required voltage BATT+ is provided by the battery.

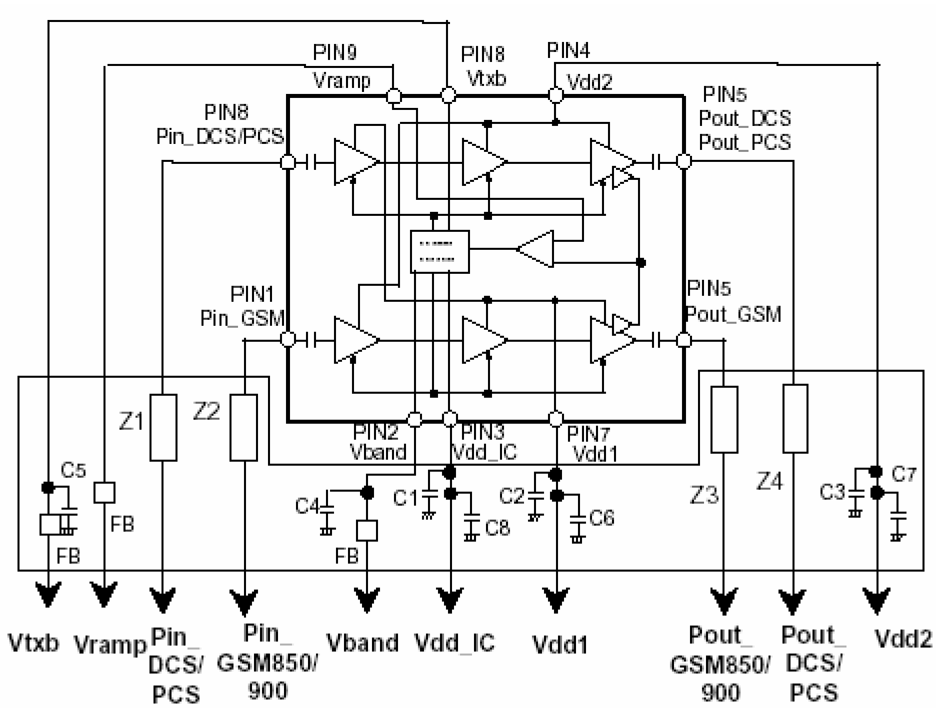
Circuit diagram



Top View

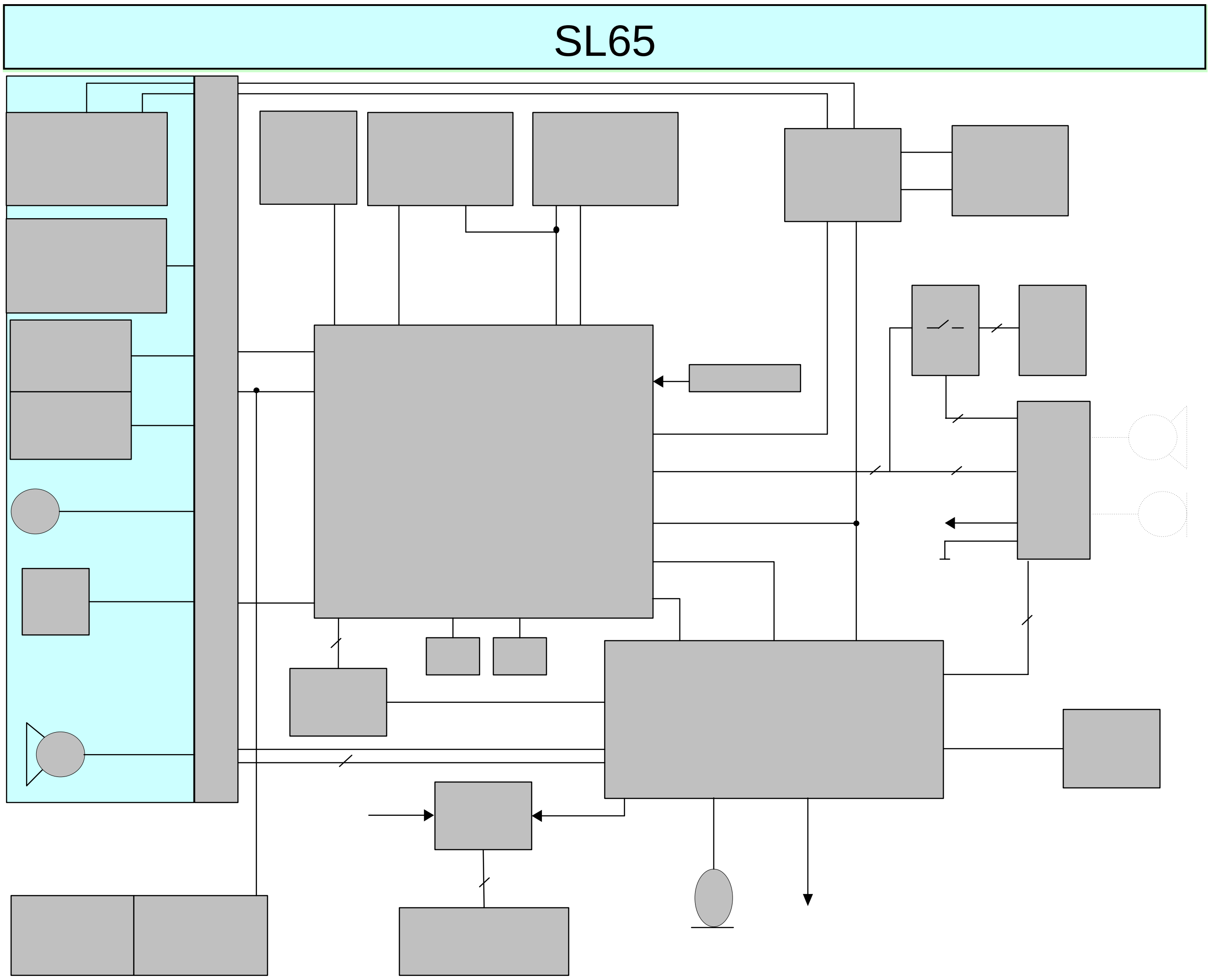


Block Diagram



5 Logic / Control

5.1 Logic Block Diagram SL65



5.2 SGOLDLITE

5.2.1 Digital Baseband

Baseband Processor SGOLDlite (PMB8875)
S-GOLDliteTM is a GSM single chip mixed signal baseband IC containing all analog and digital functionality of a cellular radio. The integrated circuit contains a ARM926EJ-S CPU and a TEAKLite DSP core. The ARM926EJ-S is a powerful standard controller and particularly suited for wireless systems. It is supported by a wide range of tools and application SW. The TEAKLite is an established DSP core for wireless applications with approved firmware for GSM signal processing. The package is a P-LFBGA-345 (264 functional pins + 81 thermical balls).

Supported Standards
- GSM speech FR, HR, EFR and AMR-NB
- GSM data 2.4kbit/s, 4.8kbit/s, 9.6kbits, and 14.4kbit/s
- HSCSD class 10
- GPRS class 12

Processing cores
- ARM926EJ-S 32-bit processor core with operating frequency up to 125 MHz for controller functions
- TEAKLite DSP core with operating frequency 104 MHz.

ARM-Memory
- 8 kByte Boot ROM on the AHB
- 96 kByte SRAM on the AHB, flexibly usable as program or data RAM
- 8 kByte Cache for Program (internal)
- 8 kByte tightly coupled memory for Program (internal)
- 8 kByte Cache for Data (internal)
- 8 kByte tightly coupled memory for Data (internal)

TEAKLite-Memory
- 80 kwords Program ROM
- 4 kwords Program RAM
- 48 kwords Data ROM
- 27 kwords Data RAM

Shared Memory Blocks
- 1.5 kwords Shared RAM (dual ported) between controller system and TEAKLite.

Functional Hardware blocks

- CPU and DSP Timers
- Programmable PLL with additional phase shifters for system clock generation
- GSM Timer Module that off-loads the CPU from radio channel timing
- GMSK Modulator according to GSM-standard 05.04 (5/2000)
- Hardware accelerators for equalizer and channel decoding
- Advanced static and dynamic power management features including TDMA-Frame synchronous low-power mode and enhanced CPU modes (idle and sleep modes)

Interfaces and Features

- Keypad Interface for scanning keypads up to 6 rows and 4 columns
- Pulse Number Modulation output for Automatic Frequency Correction (AFC)
- Serial RF Control Interface; support of direct conversion RF
- 2 USARTs with autobaud detection and hardware flow control
- IrDA Controller integrated in USART0 (with IrDA support up to 115.2 kbps)
- 1 Serial Synchronous SPI compatible interfaces in the controller domain
- 1 Serial Synchronous SPI compatible interface in the TEAKLite domain
- I2C-bus interface (e.g. connection to S/M-Power)
- 2 bidirectional and one unidirectional I2S interface accessible from the TEAKLite
- USB V1.1 mini host interface for full speed devices with up to 5 interfaces and 10 endpoints configurable supporting also USB on-the-go functionality
- ISO 7816 compatible SIM card interface
- Enhanced digital (phase linearity, adj/ co-channel interference) baseband filters, including analog prefilters and high resolution analog-to-digital converters.
- Separate analog-to-digital converter for various general purpose measurements like battery voltage, battery, VCXO and environmental temperature, battery technology, transmission power, offset, onchip temperature, etc.
- Ringer support for highly oversampled PDM/PWM input signals for more versatility in ringer tone generation
- RF power ramping functions
- DAI Interface according to GSM 11.10 is implemented via dedicated I2S mode
- 26 MHz master clock input
- External memory interface:
  - 1.8V interface
  - Data bus: 16 bit non-multiplexed and multiplexed, 32 bit multiplexed
  - Supports synchronous devices (SDRAMs and Flash Memory) up to 62.4 MHz
  - For each of the 4 address regions 128 MByte with 32-bit access or 64 MByte with a 16-bit access are addressable
  - Supports asynchronous devices (i.e. SRAM, display) including write buffer for cache line write
- Port logic for external port signals
- Comprehensive static and dynamic Power Management
  - Various frequency options during operation mode
  - 32 kHz clock in standby mode
  - Sleep control in standby mode

- RAMs and ROMs in power save mode during standby mode
- Additional leakage current reduction in standby mode possible by switching off the power for the TEAKLite subsystem.

Baseband receive path
In the receiver path the antenna input signal is converted to the base band, filtered, and amplified to target level by the RF transceiver chipset. The resulting differential I and Q baseband signals are fed into the S-GOLDliteTM. The A-to-D converter generates two 6.5 Mbit/s data streams. The decimation and narrowband channel filtering is done by a digital baseband filter for each path. The DSP performs for GMSK, the complex baseband signal equalization and the channel decoding. The recovered digital speech data is fed into the speech decoder (D1300). The S-GOLDlite supports fullrate, halfrate, enhanced fullrate and adaptive multirate speech codec algorithms.

Baseband transmit path
In the transmit direction the microphone signal is amplified and A-to-D converted by the D1300. The prefiltered and A-to-D converted voice signal passes a digital decimation filter. Speech and channel encoding (including voice activity detection, VAD, and discontinuous transmission, DTX) as well as digital GMSK modulation is carried out by the S-GOLDliteTM. The digital I and Q baseband components of the GMSK modulated signals (48-times oversampled with 13 MSamples/s) are D-to-A converted. The analog differential baseband signals are fed into the RF transceiver chipset. The RF transceiver modulates the baseband signal using a GMSK modulator. Finally, an RF power module amplifies the RF transmit signal to the required power level. The S-GOLDliteTM controller software controls the gain of the power amplifier by predefined ramping curves (16 words, 11 bit). The S-GOLDliteTM communicates with the RF chip set via a serial data interface.

The following algorithms and a task scheduler are implemented on the DSP:
Algorithms running on the DSP:

- scanning of channels, i.e, measurement of the field strengths of neighbouring base stations
- detection and evaluation of Frequency Correction Bursts
- equalisation of GMSK Normal Bursts and Synchronisation Bursts with bit-by-bit soft-output
- Synch burst channel decoder
- channel encoding and soft-decision decoding for fullrate, enhanced-fullrate and adaptive multirate speech, and control channels as well as RACH, PRACH
- channel encoding for GPRS coding schemes (CS1-CS4) as well as USF detection algorithms for the Medium Access Control (MAC) software layer
- fullrate, enhanced fullrate and adaptive multirate speech encoding and decoding
- support for fullrate (F9.6, F4.8, and F2.4) data channels

- mandatory sub-functions like
  – discontinuous transmission,
  – voice activity detection, VAD
  – background noise calculation
- generation of tone and side tone
- hands-free functions (acoustic echo cancellation, noise-reduction)
- support for voice memo
- support for voice dialling
- handling of vocoder and voice-paths for type approval testing
- ADPCM encoder (8 kHz sampling frequency), cannot run in parallel to a speech codec
- ADPCM decoder (8 kHz and 16 kHz sampling frequency), cannot run in parallel to a speech codec

Scheduler functions on the DSP:
The scheduler is based on an operating system. It is basically triggered by interrupts generated by hardware peripherals or commands from the micro-controller.

- communication between DSP and micro-controller
- fully automatic handling of speech channels
- semi-automatic handling of control channels
- support of the GSM ciphering algorithm (A51, A52, A53) in combination with the hardware accelerator.
- support for General Packet Radio Services (GPRS) with up to 4 Rx and 1Tx or 3 Rx and 2 Tx (Class 10 mobile).
- monitoring of paging blocks for packet switched and circuit switched services simultaneously GPRS MS in Class-B mode of operation
- MMS support
- loop-back functions (according to GSM 11.10)

Real Time Clock
The real time clock (degree of accuracy 150ppm) is powered via a separate voltage regulator inside the ASIC. Via a capacitor, data is kept in the internal RAM during a battery change for at least 30 seconds. An alarm function is also integrated with which it is possible to switch the phone on and off.

Measurement of Battery voltage, Battery Type and Ambient Temperature
The voltage equivalent of the temperature and battery code on the voltage separator will be calculated as the difference against a reference voltage of the S-GOLDlite. Inside the S-GOLDlite are some analog to digital converters. These are used to measure the battery voltage, battery code resistor and the ambient temperature.

Timing of the Battery Voltage Measurement
Unless the battery is being charged, the measurement shall be made in the TX time slot. During charging it will be done after the TX time slot.

5.2.2 SDRAM

Memory for volatile data. SDRAM= synchronous High data rate Dynamic RAM

Memory Size:	64 Mbit
Data Bus:	16 Bit
Frequency:	105 MHz
Power supply:	1.8 V

5.2.3 FLASH

Non-volatile but deletable and re-programmable (software update) program memory for the S-GOLDlite and for saving e.g. user data (menu settings), voice band data (voice memo), mobile phone matching data, images etc.. There is a serial number on the flash which cannot be changed.

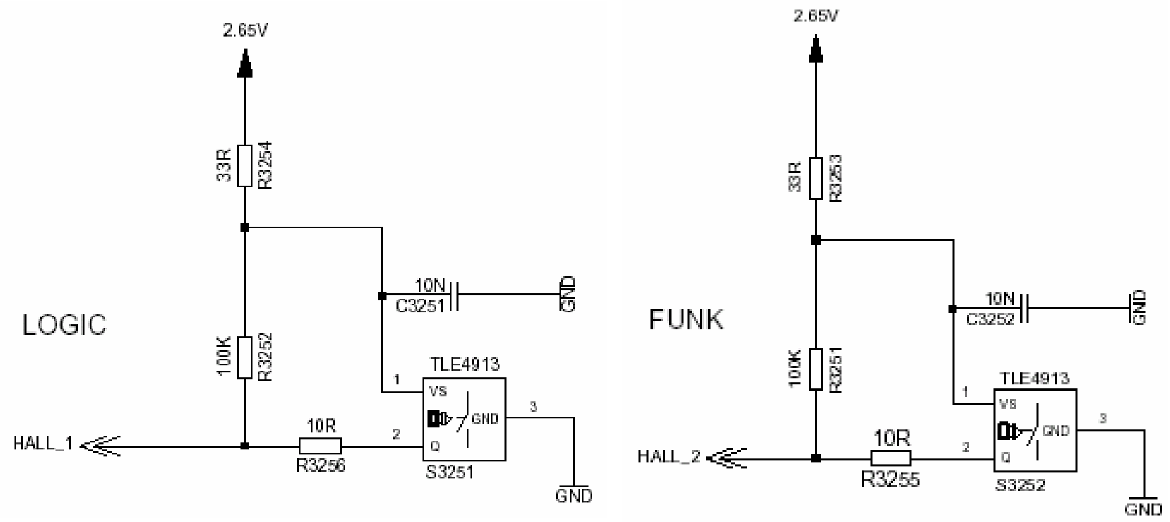
Memory Size	256 Mbit (32 MByte)
Data Bus:	16 Bit
Access Time:	Initial access: 85 ns
Synchronous Burst Mode:	54 MHz / 14ns clock to data output
Asynchronous Mode:	85 ns

5.2.4 SIM

SIM cards with supply voltages of 1.8V and 3V are supported. 1.8V cards are supplied with 3V.

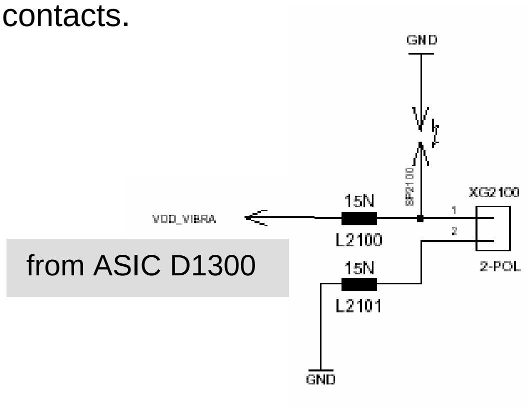
5.2.5 Hall sensor + magnet

To identify the position of the slider, 2 Hall-sensors (S3251 lower position/S3532 upper position) are placed on the PCB, and 1 Magnet in implemented in the upper case.



5.2.6 Vibration Motor

The vibration motor is mounted in the lower case. The electrical connection to the PCB is realised with pressure contacts.



6 Power Supply

6.1 ASIC Mozart / Twigo4

The power supply ASIC will contain the following functions:

- Powerdown-Mode
- Sleep Mode
- Trickle Charge Mode
- Power on Reset
- Digital state machine to control switch on and supervise the uC with a watchdog
- 17 Voltage regulators
- 2 internal DC/DC converters (Step-up and Step-down converter)
- Low power voltage regulator
- Additional output ports
- Voltage supervision
- Temperature supervision with external and internal sensor
- Battery charge control
- TWI Interface (I^2C interface)
- Bandgap reference
- High performance audio quality
- Audio multiplexer for selection of audio input
- Audio amplifier stereo/mono
- 16 bit Sigma/Delta DAC with Clock recovery and I^2S Interface

6.1.1 Battery

As a standard battery a LiIon battery with a nominal capacity 750mAh will be provided.

6.1.2 Charging Concept

6.1.2.1 General

The battery is charged in the phone. The hardware and software is designed for LiIon with 4.2V technology. Charging is started as soon as the phone is connected to an external charger. If the phone is not switched on, then charging shall take place in the background (the customer can see this via the "Charge" symbol in the display). During normal use the phone is being charged (restrictions: see below). Charging is enabled via a PMOS switch in the phone. This PMOS switch closes the circuit for the external charger to the battery. The processor takes over the control of this switch depending on the charge level of the battery, whereby a disable function in the ASIC hardware can override/interrupt the charging in the case of over voltage of the battery
For controlling the charging process it is necessary to measure the ambient (phone) temperature and the battery voltage. The temperature sensor will be an NTC resistor with a nominal resistance of 22kΩ at 25°C. The determination of the temperature is achieved via a voltage measurement on a voltage divider in which one component is the NTC. Charging is ongoing as long the temperature is within the range +5°C to 45°C. The maximal charge time will be 2 hours (I_{max}=750mA).

6.1.2.2 Measurement of Battery voltage, Battery Type and Ambient Temperature

The voltage equivalent of the temperature and battery code on the voltage separator will be calculated as the difference against a reference voltage of the S-GOLDlite. Inside the S-GOLDlite are some analog to digital converters. These are used to measure the battery voltage, battery code resistor and the ambient temperature.

6.1.2.3 Timing of the Battery Voltage Measurement

Unless the battery is being charged, the measurement shall be made in the TX time slot. During charging it will be done after the TX time slot.

6.1.2.4 Recognition of the Battery Type

The different batteries will be encoded by different resistors within the battery pack itself.

6.1.2.5 Charging Characteristic of Lithium-Ion Cells

LiIon batteries are charged with a U/I characteristic, i.e. the charging current is regulated in relation to the battery voltage until a minimal charging current has been achieved. The maximum charging current is given by the connected charger. The battery voltage may not exceed 4.2V ±50mV average. During the charging pulse current the voltage may reach 4.3V. The temperature range in which charging of the phone may be performed is in the ranges from 0...50°C. Outside this range no charging takes place, the battery only supplies current.

6.1.2.6 Trickle Charging

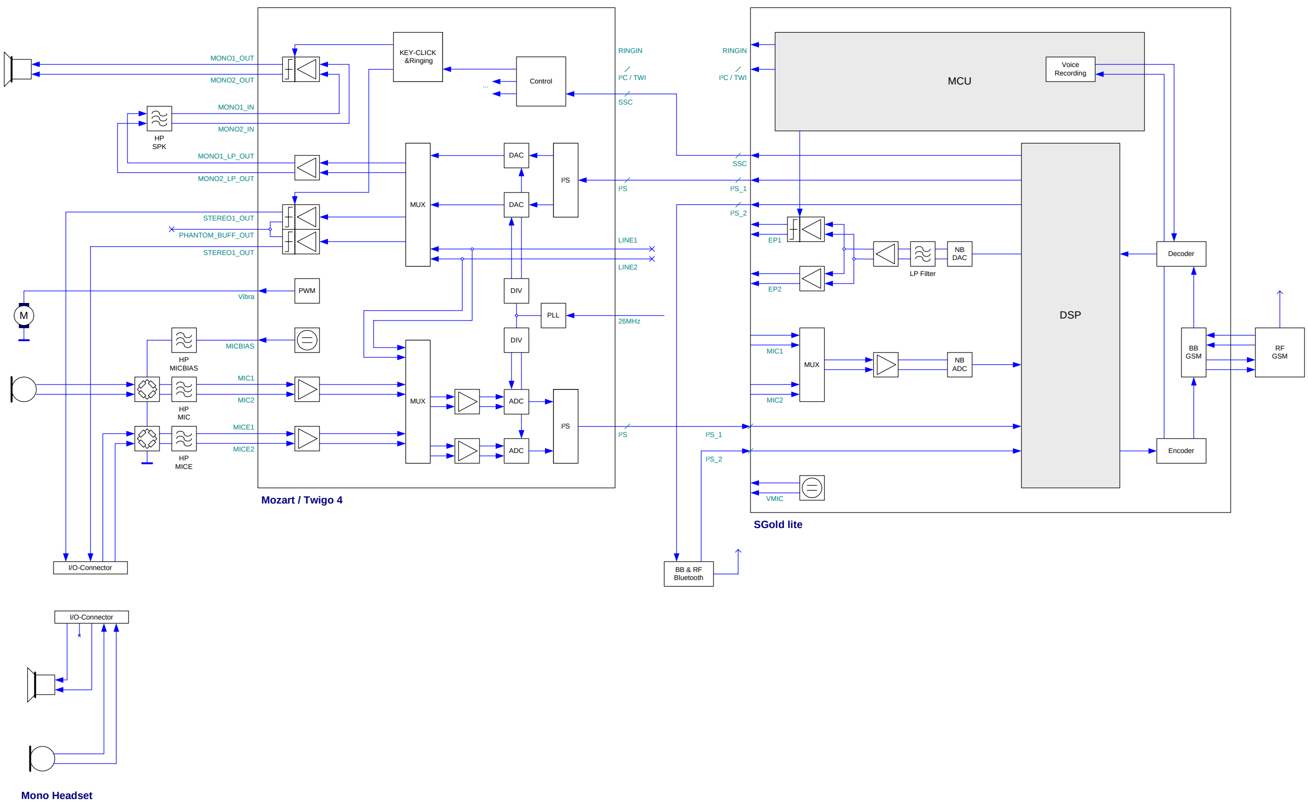
The ASIC is able to charge the battery at voltages below 3.2V without any support from the charge SW. The current will by measured indirectly via the voltage drop over a shunt resistor and linearly regulated inside the ASIC by means of the external FET. The current level during trickle charge for voltages <2.8V is in a range of 20-50mA and in a range of 50-100mA for voltages up to 3.2V. To limit the power dissipation of the dual charge FET the trickle charging is stopped in case the output voltage of the charger exceeds 10 Volt. The maximum trickle time is limited to 1 hour. As soon as the battery voltage reaches 3.2 V the ASIC will switch on the phone automatically and normal charging will be initiated by software.

6.1.2.7 Normal Charging (Fast charge)

For battery voltages above 3.2 Volt and normal ambient temperature between 0 and 50°C the battery can be charged with a charge current up to 1C. This charging mode is SW controlled and starts if an accessory (charger) is detected with a supply voltage above 6.4 Volt by the ASIC ASIC. The level of charge current is only limited by the charger.

6.1.2.8 Audio multiplexer

The digital audio information from/to the DSP inside the SGOLD are delivered via the I2S interface, the 26MHz from the RF part. The internal AD and DA converter are connected to microphone and loudspeaker.



6.1.2.9 Interface

The ASIC has two serial control interfaces and one serial audio interface. With the serial interfaces, all functions of the ASIC can be controlled. For time critical commands (all audio functions incl. Vibra) the SSC is used.

TWI interface
TWI (two wire interface) is an I2C 2 wire interface with the signals Clock (I2C_CLK) data line (I2C_DAT) and the interrupt (PM_INT).

SSC interface
The SSC interface enables high-speed synchronous data transfer between SGOLD and ASIC.
The interface consist of: clock signal (PM_SSC_SCLK), master transmit slave receive (PM_SSC_MTSR), master receive slave transmit (PM_SSC_MTSR) and the select line (PM_SSC_CS)

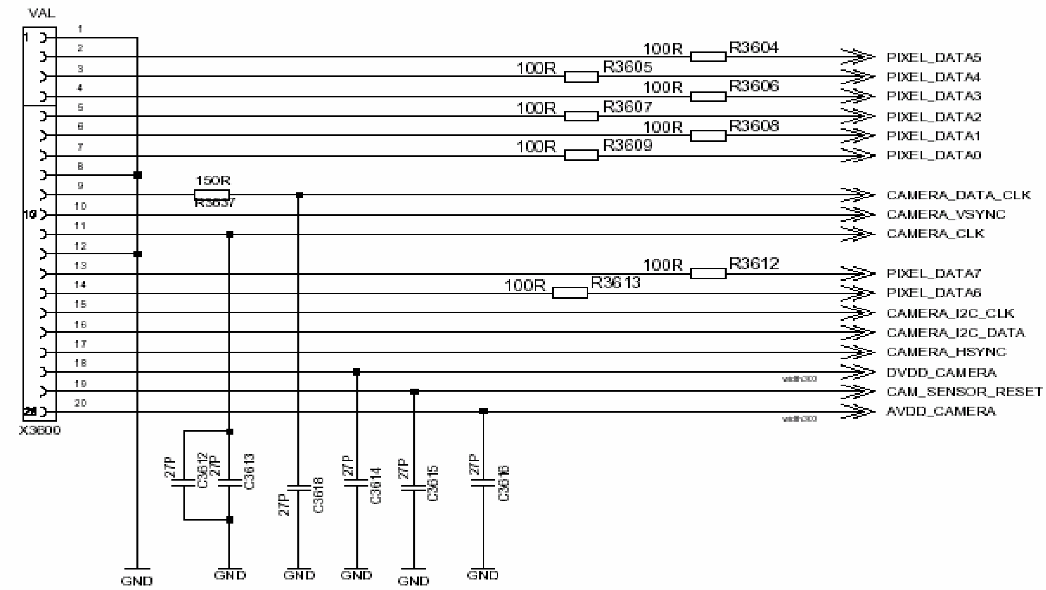
IS2 interface
The audio interface is a bidirectional serial interface, TX and RX part are independent. The IS2 interface consist of a three wire connection for each direction. The three lines are clock (CLK), the serial data line (DAC or ADC) and the word select line (WAO). Clock and word select line is used for RX and TX together in SL65. (PM_I2S_DAC for RX and PM_I2S_ADC for TX)

6.1.2.10 LDO`S

LDO´s:	*Voltage*	*Current*	*Name*	*voltage domains*
REG 1	**2,9V**	0...140mA	2.9V	Display, Epson Camera-Chip, SGOLD
REG 2a	**1,5V**	0...300mA	1.5V_UC	SGOLD
REG 2b	**1,5V**	0...100mA	1.5V_DSP	SGOLD
REG 3	**2,65V**	0...140mA	2.65V	SGOLD, Hall-Sensor, Epson Camera-Chip, USB Switch
MEM REG1	**1,8V**	0...250mA	1.8V_MEM1	SGOLD, Display, SDRAM
MEM REG2	**1,8V**	0...150mA	1.8V_MEM2	Flash Memory, Camera-ASIC
AUDIO REG	**2,9V**	0...190mA	VAUDREGA	PMU ASIC
RF REG1	**2,7V**	0...150mA	VDD_RF1	RF-Part (Hitachi Bright V)
AFC REG	**2,65V**	0...2mA	VDD_AFC	SGOLD
LP_REG	**2,0V**	0...2mA	VDD_RTC	SGOLD
SIM REG	**2,9V**	0...70mA	VDD_SIM	SIM
USB REG	**3,1V**	0...40mA	VDD_USB	SGOLD, USB Protection
VIBRA	**2,8V**	0...140mA	VDD_VIBRA	VIBRA

7 Camera

The camera module uses a colour sensor with a full VGA (640x480) resolution in landscape orientation. The module will deliver an 8Bit output signal which will be pre-processed by the EPSON S1D13716 graphic engine chip. Various settings like brightness, image stabilization, white balance can be done by using the I2C interface.



8 Camera – Display Interface Module

For the interface between S-GOLDlite, camera and display a graphics engine chip called S1D13716 from Epson is used. By using the SSC interface the S-GOLDlite communicates with this graphic engine chip. The S1D13716 has a second SSC interface to adapt the display. Over an I2C interface, provided by the S1D13716, the camera-module can be initialised; the picture-data output of the camera goes over a parallel 8-bit interface

There are three modes available:

a) Bypass mode:

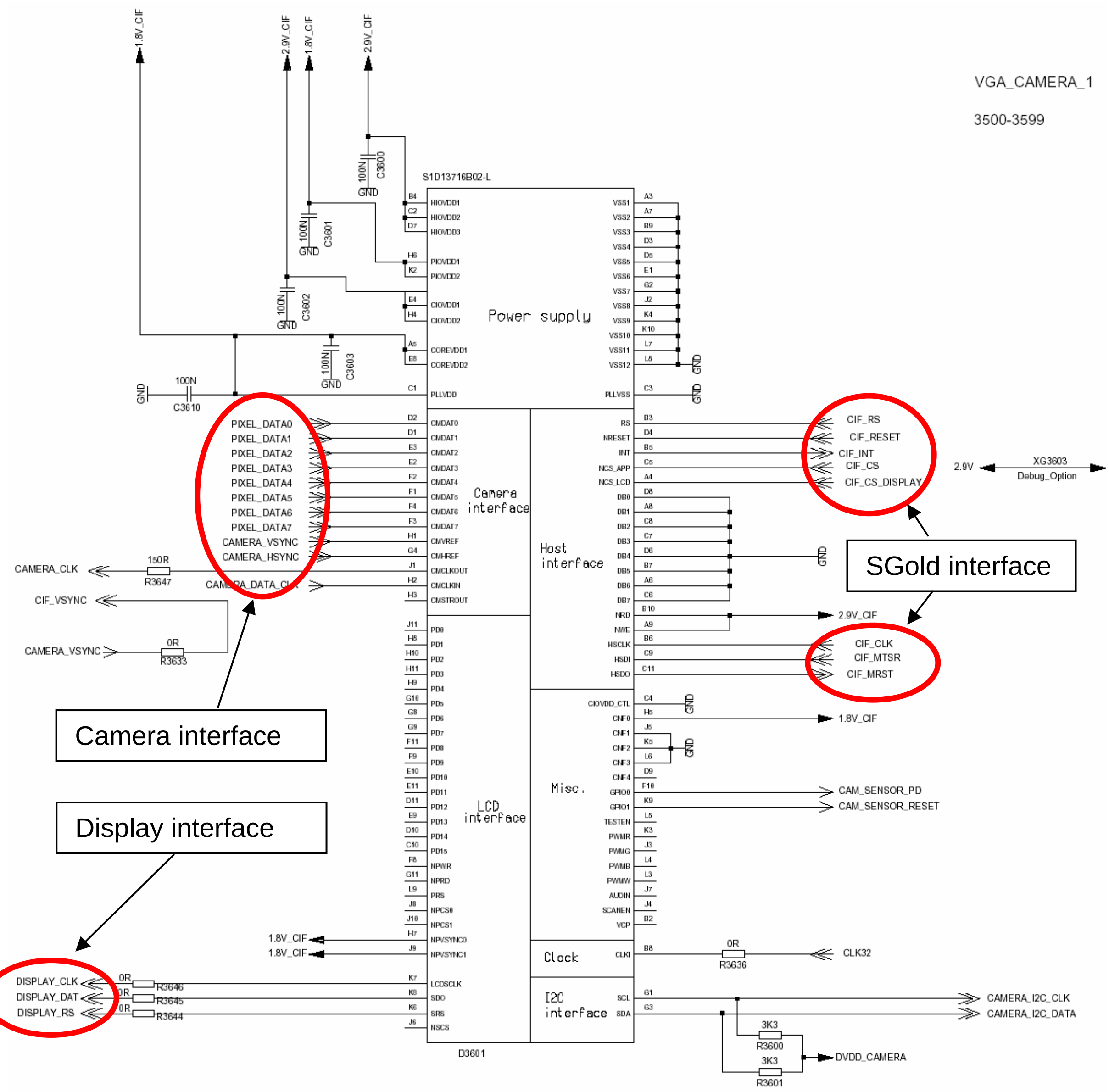
In this mode the S1D13716 is transparent regarding the display. The S-GOLDlite communicates “directly” with the display.

b) Camera View Mode:

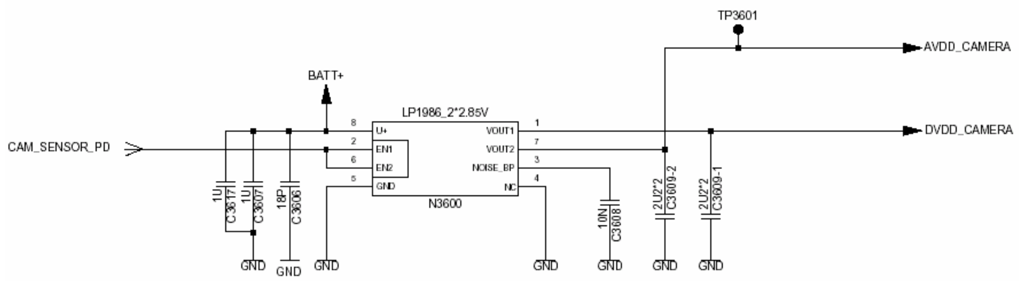
In this mode the S1D13716 transfers the picture – data from the camera directly to the display. A resizing and compressing engine is available to reduce the data amount to the display. So the preview can be done without using the SGOD performance.

c) Camera Capture Mode:

In this mode the picture – data from the camera is sent to the SGOLD. There are resizing and compressing engines available to reduce the data-stream to the SGOLD-lite

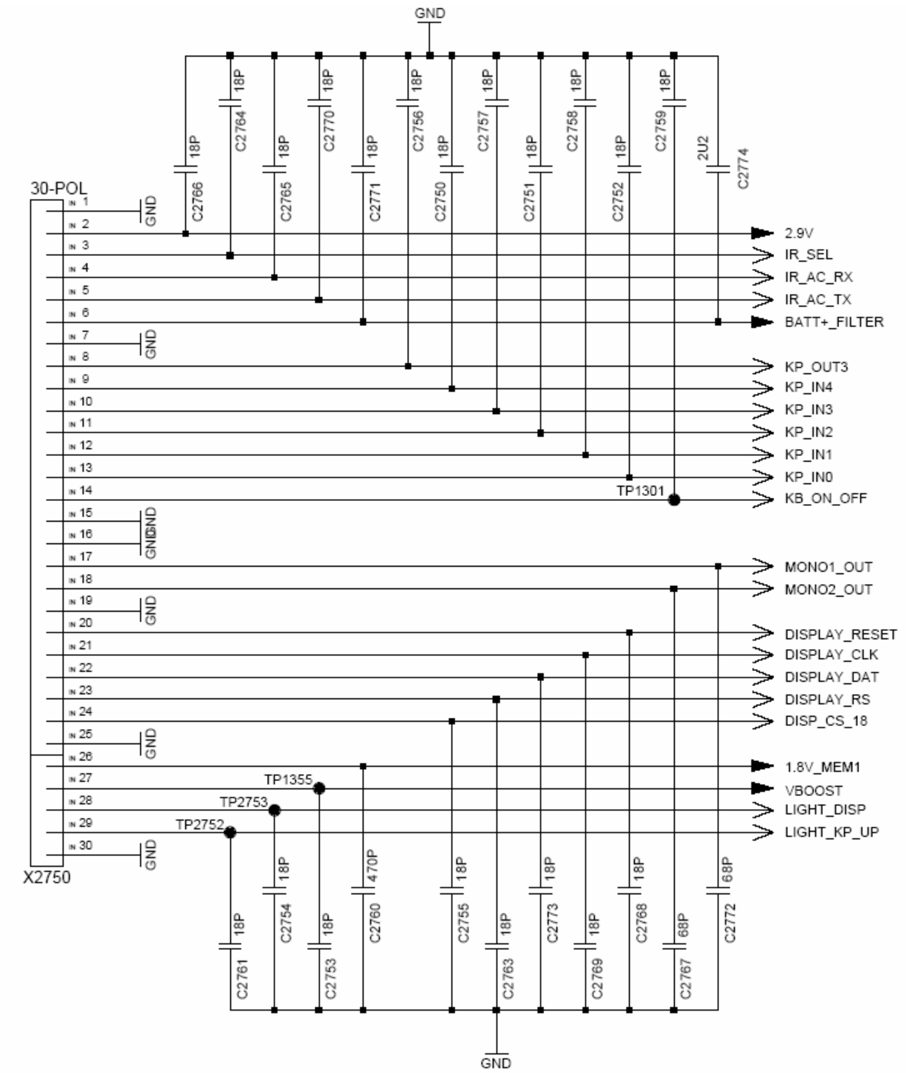


Voltage supply for Camera Asic

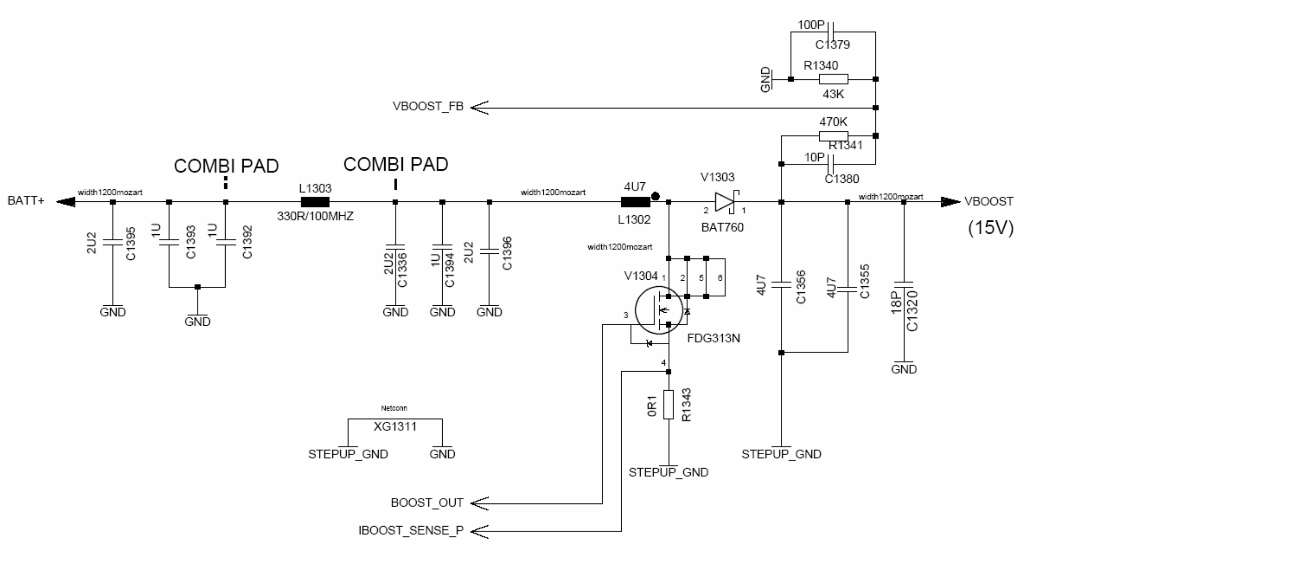


9 Display Module

The display has a resolution of 130x130 pixels with a color depth of 65536 colors. It contains an active-matrix panel (TFD, where the colors are generated by red, green and blue color filters) and a plastic housing. The controller is directly mounted on the panel of the display. In order to guarantee a very efficient illumination the white LEDs are mounted on a flex foil inside the module. In addition, all passive components necessary to drive an LCD are also assembled on this flex foil. Thus, the only interconnections to the Siemens MMI PCB are the data lines and the power supply lines of the controller and the white LEDs. The MMI pcb itself will be connected to the main pcb by flex with BB connector (30pins).



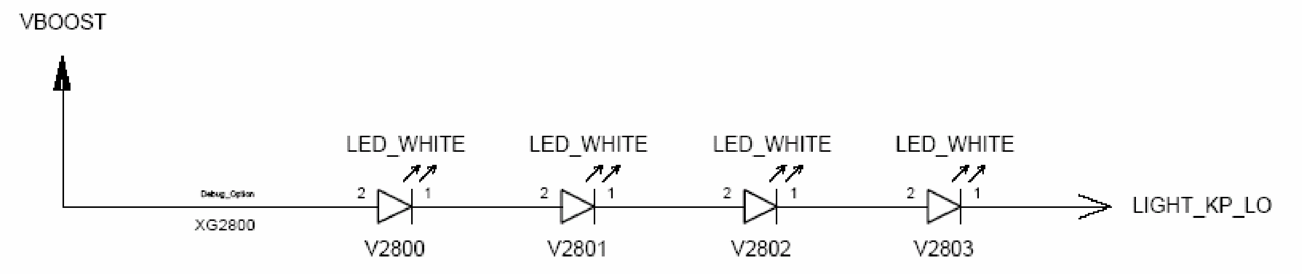
The display controller is being driven with a supply voltage of VDD1_2.9V = 2.90 V and VDD2_1.8V=1.8 V. The 3 white side-shooter LEDs are driven in serial. The maximum current is 15mA. The voltage for the 3 LEDs is VDD_Boost.



10 Illumination

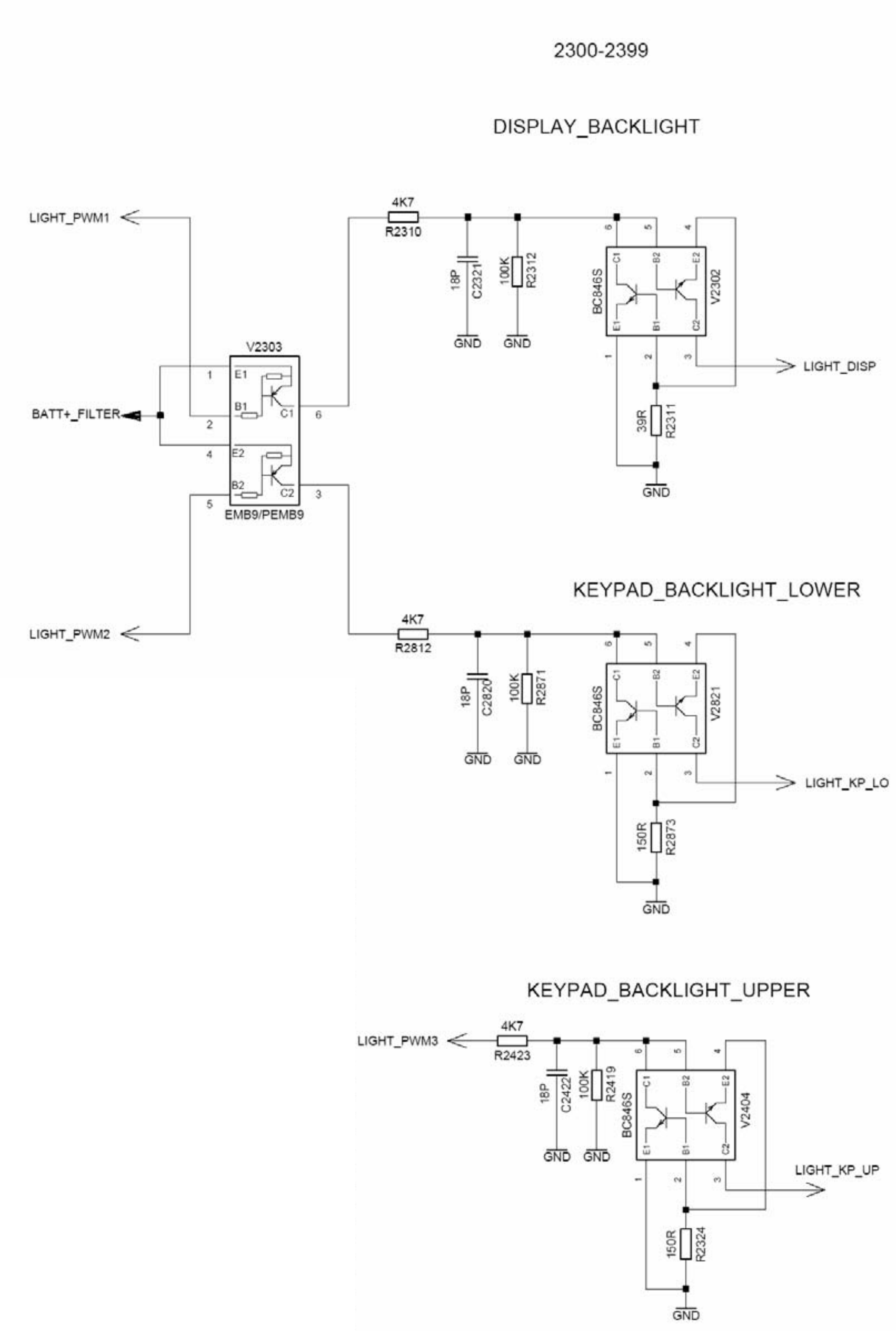
a) Keyboard

The LED´s will be mounted on separate MMI-PCB. The illumination of the keypad will be done via high-brightness LEDs (colour: white, type: top-shooter, driven by 7.5 mA / LED). The LEDs will be driven by one current source with a maximum current of 15 mA. The 6 LEDs are divided in two groups with 3 LEDs in serial.



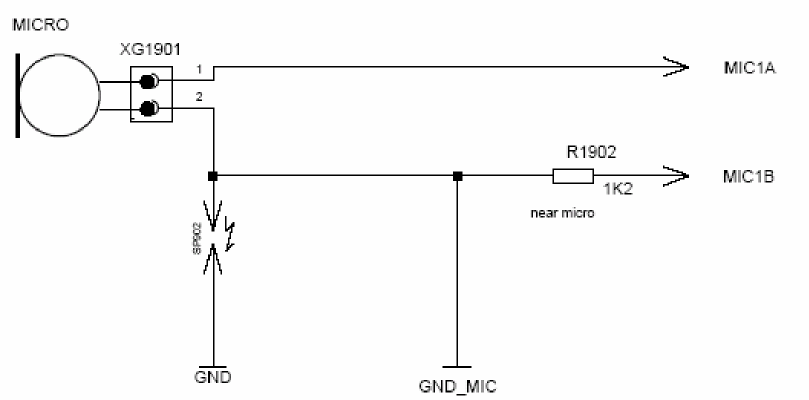
b) Display

The 3 serial LEDs for the display are supplied by one constant current sources, to ensure the same brigthness and colour of the white backlight.


2300-2399
DISPLAY_BACKLIGHT
LIGHT_PWM1
4K7
R2310
18P
C2321
100K
R2312
GND
BC846S
V2302
LIGHT_DISP
V2303
BATT+_FILTER
EMB9/PEMB9
39R
R2311
KEYPAD_BACKLIGHT_LOWER
LIGHT_PWM2
4K7
R2812
18P
C2820
100K
R2871
V2821
LIGHT_KP_LO
150R
R2873
KEYPAD_BACKLIGHT_UPPER
LIGHT_PWM3
4K7
R2423
18P
C2422
100K
R2419
V2404
LIGHT_KP_UP
150R
R2324

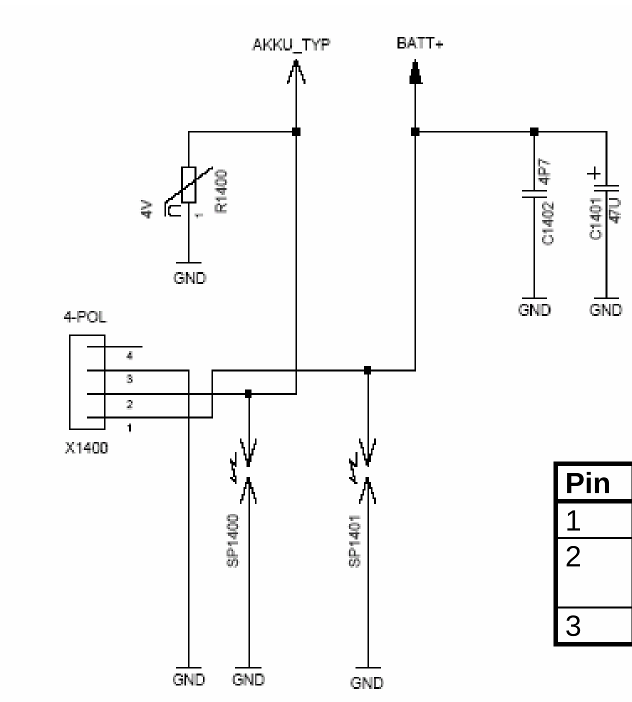
11 Interfaces

11.1 Microphone



Pin	Name	IN/OUT	Remarks
1	MIC1A	O	Microphone power supply. The same line carries the low frequency speech signal.
2	MIC1B		GND_MIC

11.2 Battery



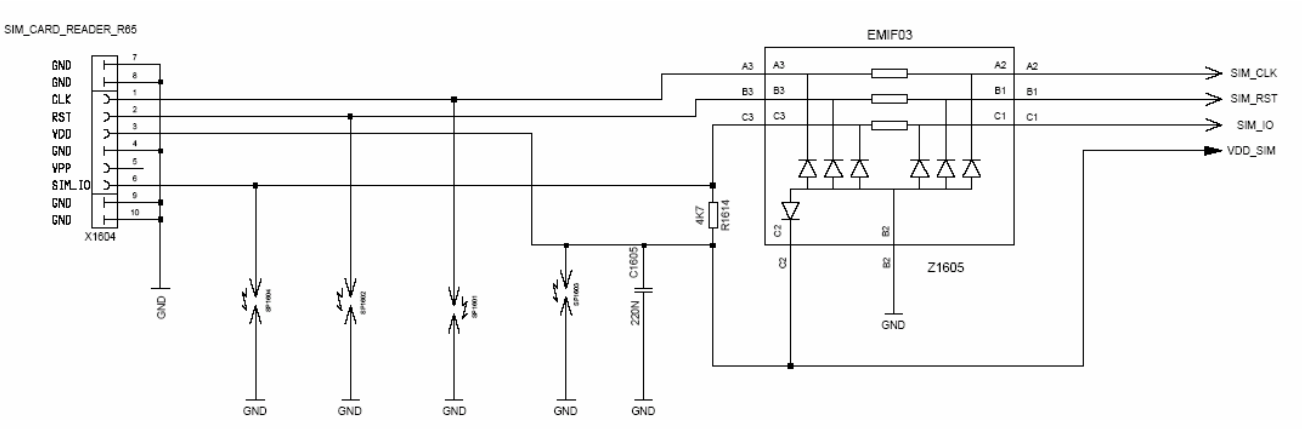
Pin	Name	Level	Remarks
1	GND	-	Ground
2	AKKU_TYP	0V...2.65V	Recognition of battery/supplier
3	BATT+	3 V... 4.5V	Positive battery pole

11.3 IRDA

A Low-Power infrared data interface, compatible to "IrDA - Infrared Data Association; Serial Infrared Physical Layer Specification, Version 1.3", supporting transmission rates up to 115.2kbps (Slow IrDA) will be provided. As a Low-Power-Device, the infrared data interface has a transmission range of at least:

- 20cm to other Low-Power-Devices and
- 30cm to Standard-Devices

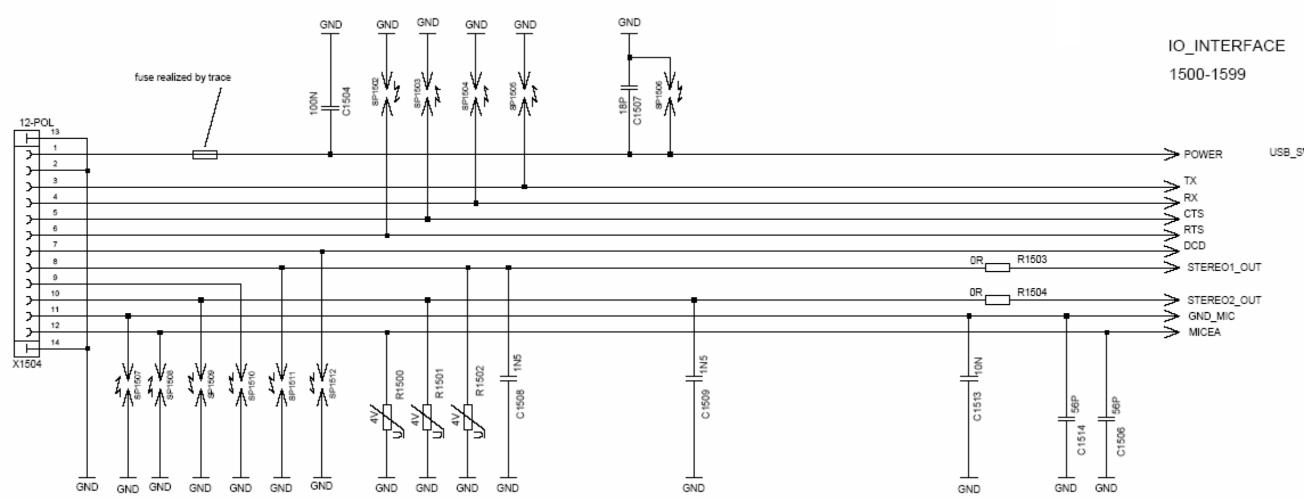
11.4 Interface SIM Module



Pin Name	IN/OUT	Remarks
SIM_CLK	O	Pulse for chipcard. The chipcard is controlled directly from the SGOLD+.
SIM_RST	O	Reset for chipcard
SIM_IO	I O	Data pin for chipcard; 4,7 kΩ pull up at the VDD_SIM pin
VDD_SIM	O	Switchable power supply for chipcard; 220 nF capacitors are situated close to the chipcard pins and are necessary for buffering current spikes.

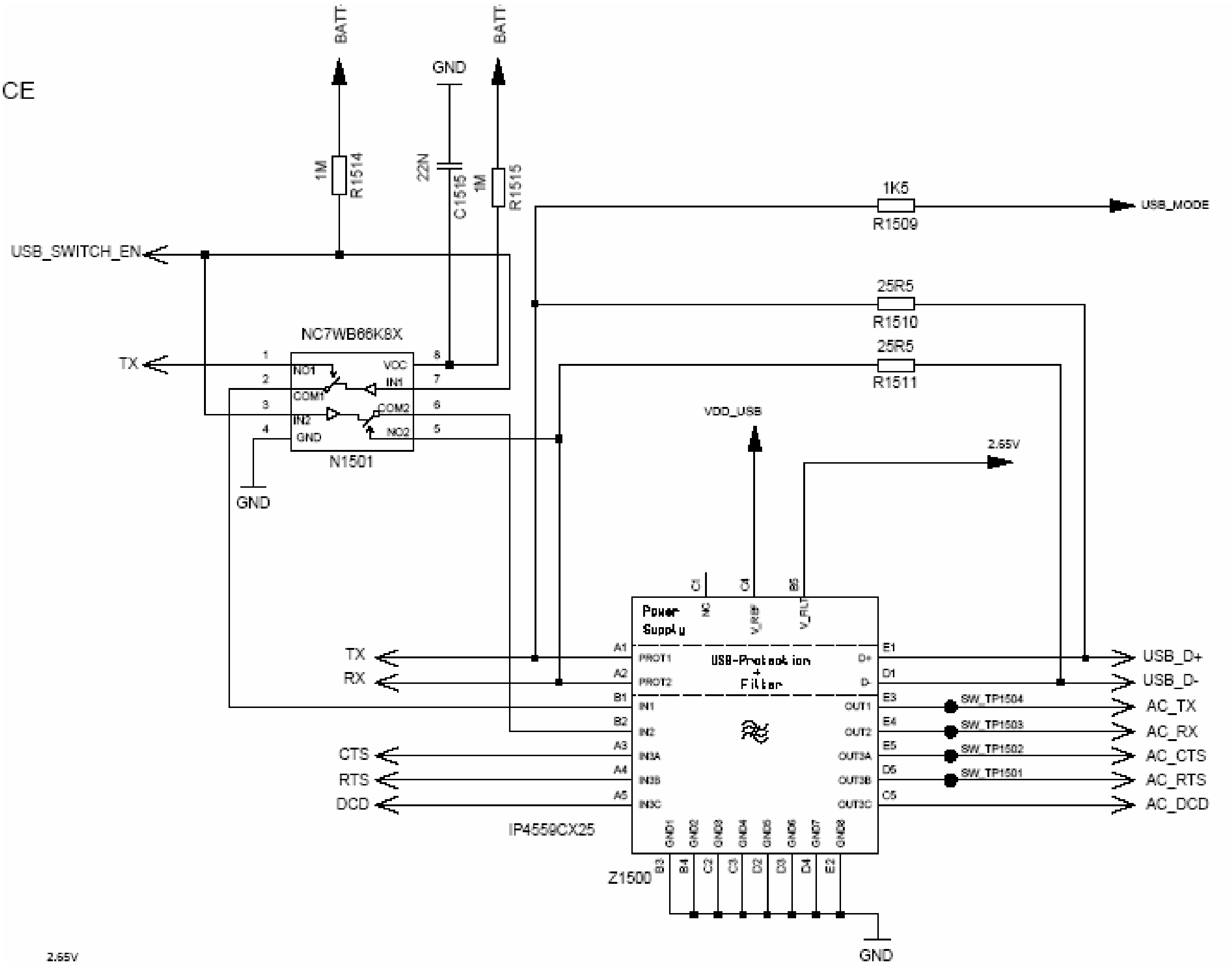
11.5 IO Connector with ESD protection

11.5.1 IO Connector – New Slim Lumberg



Pin	Name	IN/OUT	Notes
1	POWER	I/O	POWER is needed for charging batteries and for supplying the accessories. If accessories are supplied by mobile, talk-time and standby-time from telephone are reduced. Therefore it has to be respected on an as low as possible power consumption in the accessories.
2	GND		
3	TX/D+	OI/O	Serial interface USB-interface full-speed 12Mbit/s
4	RX/D-	I	Serial interface USB-interface full-speed 12Mbit/s
5	DATA/CTS	I/O	Data-line for accessory-bus Use as CTS in data operation.
6	RTS	I/O	Use as RTS in data-operation.
7	CLK/DCD	I/O	Clock-line for accessory-bus. Use as DTC in data-operation.
8	STEREO1_OUT	Analog O	driving ext. headset STEREO1_OUT and STEREO2_OUT differential mode
9	GND		
10	STEREO2_OUT	Analog O	driving ext. right to PHANTOM_BUF_OUT with mono-headset STEREO1_OUT and STEREO2_OUT differential mode
11	GND_MIC	Analog I	for ext. microphone
12	MICEA_AC	Analog I	External microphone

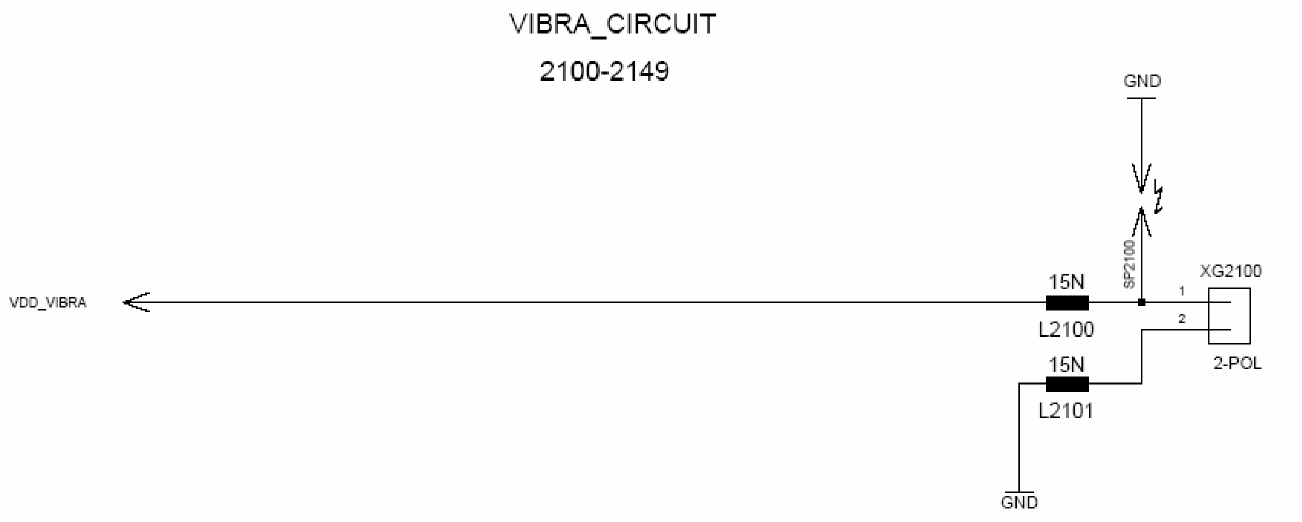
11.5.2 ESD Protection with EMI filter



The Z1500 is a 5-channel filter with over-voltage and ESD Protection array which is designed to provide filtering of undesired RF signals in the 800-4000MHz frequency band Additionally the Z1500 contains diodes to protect downstream components from Electrostatic Discharge (ESD) voltages

11.6 Vibration Motor

The vibration motor is mounted in the lower case. The electrical connection to the PCB is realised with pressure contacts



Pin	Name	IN/OUT	Remarks
1	VDD_VIBRA		Vbatt will be switched by PWM-signal with internal FET to VDD_Vibra in Asic
2	GND		

12 Keyboard

The keyboard is connected via the lines KPOUT0 – KPOUT3 and KPIN0 – KPIN4 with the SGOLDLITE. KB_ON_OFF is used for the ON/OFF switch. KP_INO is used for the side keys. KPIN4 and KPOUT0, KPOUT1, KPOUT2 are used for the side keys.