Data Sheet, Rev. 1.1, 2005-12-15

PMB6814 V1.0 E-POWERlite

Wireless Solutions

Never stop thinking.

Edition 2005-12-15

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
D-81541 München, Germany

For questions on technology, delivery and prices please contact the Infineon Technologies Offices in Germany or the Infineon Technologies Companies and Representatives worldwide: see our webpage at http://www.infineon.com.

Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (see address list).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Trademarks and Registered Terms

Bluemoon®, BlueNix®, M-GOLD®, SCT®, Sieget®, Smarti®, UCP®, WDTC® are registered trademarks of Infineon Technologies AG.

S-GOLD™, E-GOLD™ are trademarks of Infineon Technologies AG.

CONFIDENTIAL

CONFIDENTIAL

1 Introduction

1.1 Revision History

Table 1-1 Revision History

Current version	Data Sheet	Rev. 1.1, 2005-12-15
Previous version	Target Specification Data Sheet	Rev. 3.2, 2004-07-04 Rev. 1.0, 2005-10-19

Table 1-2 Changes for Data Sheet Rev. 1.1

Page/Chapter	Change
Table 6-2	Package drawing for PG-VQFN-48-15 added

1.2 Overview

PMB6814 V1.0 E-POWERlite is a highly integrated power and battery management IC for mobile handsets. The device provides all power supply functions (except for the RF PA) by minimizing external device count. It is designed for usage with:

- E-GOLDlite baseband device
- SMARTi-SD RF device

1.3 Feature Overview

- Highly efficient step-down converter for main digital baseband supply including core, DSP and memory interface (External Bus Unit).
- Support of E-GOLDlite standby power-down concept
- Low-drop-out (LDO) regulators for flash and mobile RAM memory devices
- LDO regulators for baseband I/O supply
- LDO regulator for analog mixed-signal section of E-GOLDlite
- Low-noise LDO regulators for RF devices
- Audio amplifier for hands-free operation and ringing
- Charge control for charging of NiMH and Li-Ion/Polymer batteries under software control
- Pre-charge current generator with selectable current level
- RTC regulator with ultra-low quiescent current
- Backlight LEDs driver with current selection and PWM dimming function
- Two single LED driver outputs for signalling
- Vibrator driver with adjustable voltage
- Fully controllable by software via I2C-bus

CONFIDENTIAL

- Temperature and battery voltage sensors
- Interrupt channels for peripherals
- System debug mode
- PG-VQFN 48 package with heat sink and non-protruding leads

Note: Since appropriate security functions have been implemented in E-GOLDlite no ID register is available on E-POWERlite.

Note: Since a highly versatile watch-dog timer is implemented on E-GOLDlite no watch-dog timer is available on E-POWERlite.

1.4 Feature Comments

PMB6814 V1.0 E-POWERlite is a further step on the successful E-Power product line with enhanced and optimized functionality.

E-POWERlite features a baseband supply concept with a DC/DC step-down converter (SDBB) cascaded by two linear regulators (LBB1, LBB2)

- E-POWERlite's DC/DC converter makes up to 40 % reduction of battery current possible.
- SDBB has high efficiency up to 95% and a power save mode.
- Memory interface is directly supported by the SDBB
- SDBB can also act as main supply voltage for the E-GOLDlite baseband device.
- Two linear regulators for DSP and core of E-GOLDlite are cascaded after the SDBB

E-POWERlite supports the standby power-down concept of E-GOLDlite by temporarily switching off the linear regulator LBB1 for the DSP during mobile standby. In this phase the C166 controller and most peripherals are kept powered-up with power being supplied by the other linear regulator LBB2.

E-POWERlite includes a fully differential audio amplifier

- Can drive loads down to 8 Ohm (nominal)
- Allows hands-free operation and polyphone ringing
- Programmable common mode voltage for maximum output power
- Adjustable gain
- Mute switch
- Click and pop protection

E-POWERlite also integrates a charging function for Li-Ion, Li-Polymer and NiMh batteries

- Precharge current source with two voltage levels
- Constant current / constant voltage charging with 3 different termination voltages
- Programmable charge current limitation for use with different batteries
- Freely programmable pulse charging to reduce the thermal power dissipation in the constant voltage charging phase
- Top-off charge current sensing

CONFIDENTIAL

E-POWERlite fully supports LED and vibra motor functionality

- No external components needed
- Driver for backlight LEDs adjustable in steps up to 140 mA and with soft turn on and off by PWM dimming
- Two driver outputs for single LEDs for precharge indication and signalling with i.e. change of colour
- Driver for Vibra Motor with adjustable voltages, soft startup / shutdown and current limitation

E-POWERlite offers several control functions

- Power-on reset generator with logic state machine
- I2C bus interface
- I2C bus configurable mode control logic with ON (push-button or RTC), VCXOEN
- Programmable interrupt channels to handle peripherals
- Monitoring of charging functions
- Undervoltage shut-down
- Errorflags (volatile or non-volatile) from many power-supply functions and thermal sensor in order to debug system
- Overtemperature shut-down
- Overtemperature warning
- Support of E-GOLDlite standby power-down concept
- Support of E-GOLDlite power-down pad tristate function

E-POWERlite comes in a PG-VQFN 48 package

- Minimized board footprint of 7 x 7 mm
- Superior thermal characteristics with a thermal resistance of 20 K/W typical
- Power dissipation up to 2 W can be handled

1.5 Typical Application

A functional block diagram with typical application circuitry is shown in **Figure 1-1**.

Important application information:

- In general all peripheral passive devices as shown in **Figure 1-1** must be attached to E-POWERlite to enable full function.
- If the charging function is not used pin VCHS has to be shorted to pin VBATS in any case.

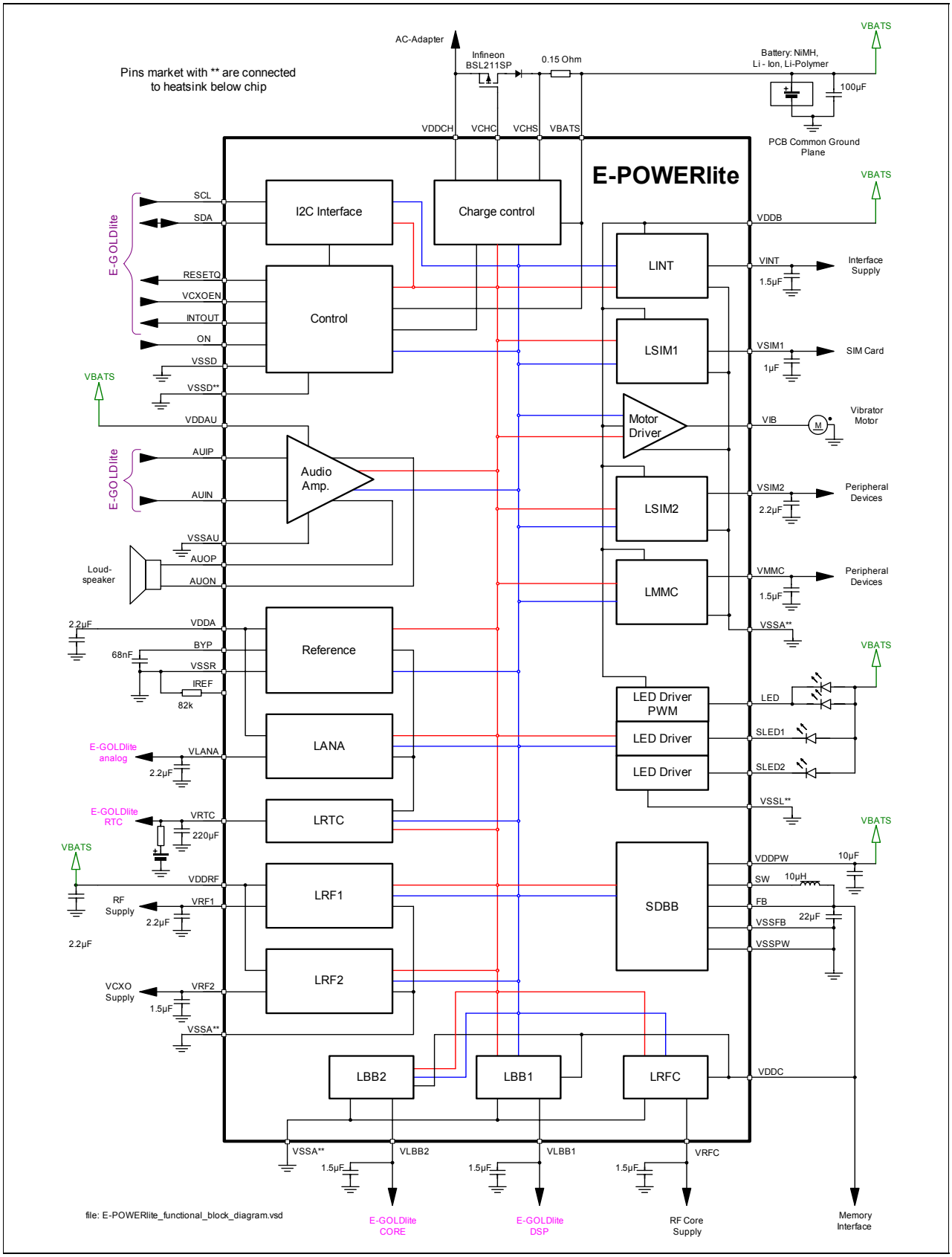

Figure 1-1 Functional Block Diagram with Typical Application Circuitry

CONFIDENTIAL

2 Pin Descriptions

2.1 Pin Diagram

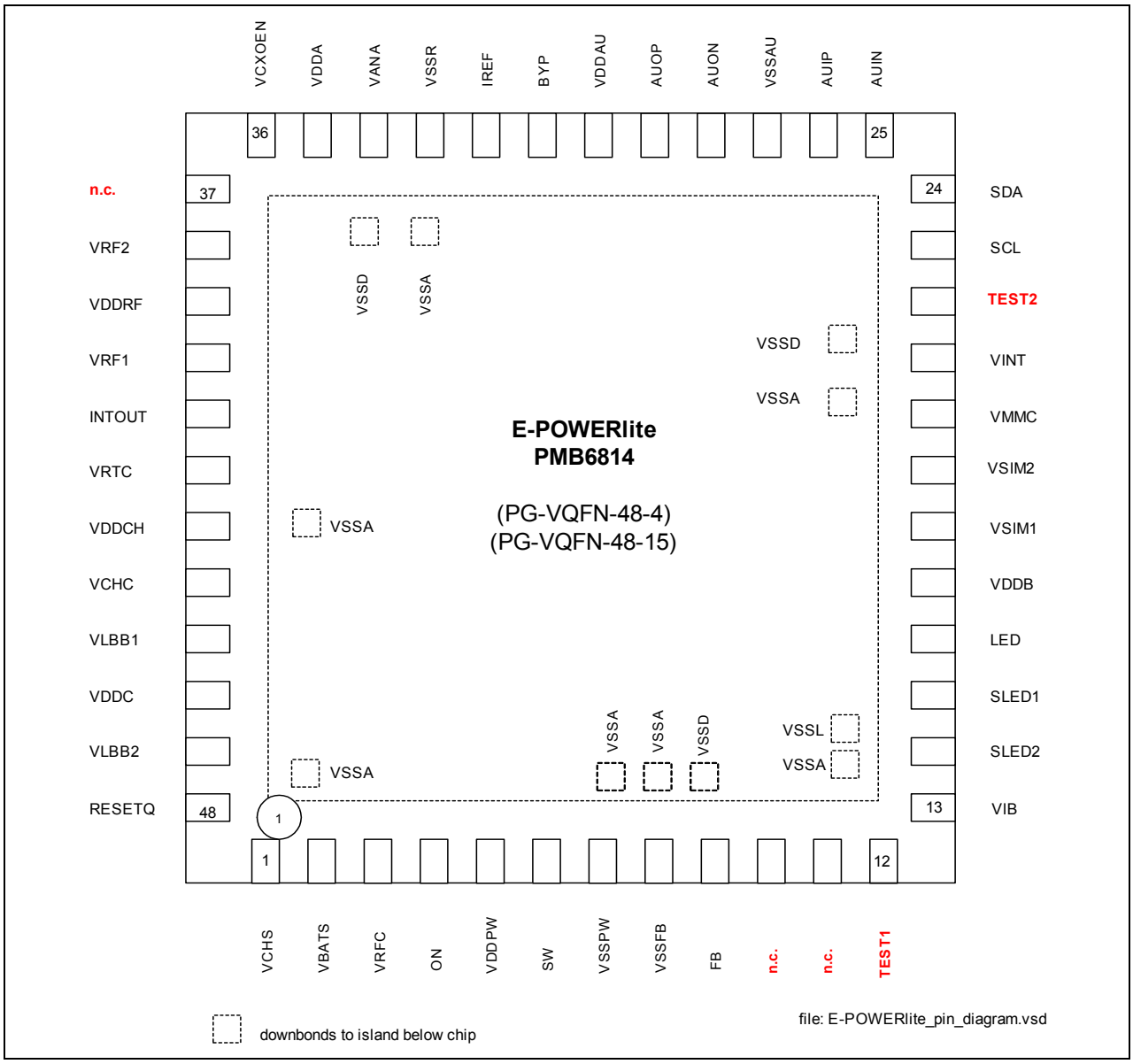

Figure 2-1 Pin Diagram of E-POWERlite (Top View)

CONFIDENTIAL

2.2 Pin Descriptions and Functions

Table 2-1 PMB6814 V1.0 E-POWERlite Pin List

Pos.	Symbol	Pin[1)] Type	Function
1	VCHS	I/O	Charge current sense / precharge output
2	VBATS	I	Battery voltage sense
3	LRFC	O	Supply for RF core
4	ON	I	Push-button or RTC power on
5	VDDPW	S	Input voltage for SDBB output stage
6	SW	O	SDBB output
7	VSSPW	S	Ground for SDBB output stage
8	VSSFB	S	Ground sense of SDBB
9	FB	I	Feedback of SDBB
10	-	-	N.c.
11	-	-	N.c.
12	TEST1	I	Test pin, connect to VSS for normal operation
13	VIB	O	Vibrator motor driver output
14	SLED2	O	Supply for second single LED
15	SLED1	O	Supply for first single LED
16	LED	O	Supply for backlight LED
17	VDDB	S	Input voltage for peripheral regulators
18	VSIM1	O	Supply for SIM Card and E-GOLDlite SIM interface
19	VSIM2	O	Supply for peripheral devices
20	VMMC	O	Supply for peripheral devices
21	VINT	O	Supply for E-GOLDlite interfaces (I2C, SSC, Keypad)
22	TEST2	S	Test pin, connect to VSS for normal operation
23	SCL	I	I2C Bus clock
24	SDA	I/O	I2C Bus data / acknowledge
25	AUIN	I	Differential audio amplifier input n from E-GOLDlite acts also as digital ringing input n
26	AUIP	I	Differential audio amplifier input p from E-GOLDlite acts also as digital ringing input p

CONFIDENTIAL

Table 2-1 PMB6814 V1.0 E-POWERlite Pin List

Pos.	Symbol	Pin[1] Type	Function
27	VSSAU	S	Ground for audio amplifier
28	AUON	O	Differential audio amplifier output n
29	AUOP	O	Differential audio amplifier output p
30	VDDAU	S	Input voltage for audio amplifier
31	BYP	O	Bypass capacitor for bandgap reference
32	IREF	O	Current reference resistor
33	VSSR	S	Ground for references
34	VANA	O	Supply for analog macro of E-GOLDlite
35	VDDA	S	Input voltage for analog regulators
36	VCXOEN	I	Mode toggling by E-GOLDlite
37	-	-	N.c.
38	VRF2	O	Supply for External Oscillator
39	VDDRF	S	Input voltage for RF regulators
40	VRF1	O	Supply for RF IC
41	INTOUT	O	Interrupt output to E-GOLDlite
42	VRTC	O	Supply for E-GOLDlite real time clock domain
43	VDDCH	S	Input voltage for charge control (from external AC-adapter)
44	VCHC	O	Control output for external PMOS device
45	VLBB1	O	Supply for E-GOLDlite DSP
46	VDDC	S	Input voltage for baseband regulators and vibrator motor driver
47	VLBB2	O	Supply for E-GOLDlite core including C166
48	RESETQ	O	Resetq output to E-GOLDlite
*	VSSA	S	5 grounds for analog circuits
*	VSSD	S	3 grounds for digital circuits
*	VSSL	S	Ground for LED drivers

[1] I : Input, O : Output, S : Supply, *: connected to island below chip

CONFIDENTIAL

2.3 Migration from SM-POWER V1.5 to E-POWERlite

2.3.1 Drop-in Replacement

Table 2-2 shows the change of pinning and application for SM-POWER V1.5 and E-POWERlite. The following issues must be obeyed for a design that supports both devices (drop-in replacement):

- LRF3EN must be connected to GND
- For stability reasons the application cirucit as proposed in the SM-POWER V1.5 data sheet should be applied to VUPU, VRF3, VUSB and VBUS.

Table 2-2 Changes in Pinout and Application

Pos.	SM-POWER V1.5	E-POWERlite		Common Application for SM-POWER V1.5 and E-POWERlite
	Symbol	Symbol	Remark	
10	VUPU	n.c.	Pin internally not connected.	Can be left unconnected for E-POWERlite. For drop-in replacement: Application as proposed for SM-POWER V1.5. When using E-POWERlite external components can be omitted.
37	VRF3	n.c.	Pin internally not connected.	
11	VUSB	n.c.	Pin internally not connected.	
12	VBUS	TEST1	Pin internally pulled to VSS. Pin only used for test purposes.[1)]	Three possibilities: 1 Connect pin to VSS. 2 Leave pin unconnected. 3 Use application as proposed for SM-POWER V1.5.
22	LRF3EN	TEST2	Pin only used for test purposes.[2)]	Connect pin to VSS.

1) Used for scan path testing.

2) Used for scan path testing.

2.3.2 Migration of Pinning SM-POWER V0.5/V1.5/E-POWERlite

Table 2-3 compares the pinning of the different POWER versions.

Table 2-3 Pin List Comparison between POWER Chips

Pos.	SM POWER V0.5	SM-POWER V1.5	E-POWER lite	Remark
1	VCHS	VCHS	VCHS	
2	VBATS	VBATS	VBATS	
3	ON	LRFC	LRFC	Difference between V0.5 and V1.5
4	VIB	ON	ON	Difference between V0.5 and V1.5
5	VDDPW	VDDPW	VDDPW	
6	SW	SW	SW	
7	VSSPW	VSSPW	VSSPW	
8	VSSFB	VSSFB	VSSFB	
9	FB	FB	FB	
10	VUPU	VUPU	---	E-POWERlite modified
11	VUSB	VUSB	---	E-POWERlite modified
12	VBUS	VBUS	TEST1	E-POWERlite modified
13	VCXOEN	VIB	VIB	Difference between V0.5 and V1.5
14	SLED2	SLED2	SLED2	
15	SLED1	SLED1	SLED1	
16	LED	LED	LED	
17	VDDB	VDDB	VDDB	
18	VSIM1	VSIM1	VSIM1	
19	VSIM2	VSIM2	VSIM2	
20	VMMC	VMMC	VMMC	
21	VINT	VINT	VINT	
22	LRF3EN	LRF3EN	TEST2	E-POWERlite modified
23	SCL	SCL	SCL	
24	SDA	SDA	SDA	
25	AUIN	AUIN	AUIN	
26	AUIP	AUIP	AUIP	
27	VSSAU	VSSAU	VSSAU	
28	AUON	AUON	AUON	
29	AUOP	AUOP	AUOP	

CONFIDENTIAL

Table 2-3 Pin List Comparison between POWER Chips

Pos.	SM POWER V0.5	SM-POWER V1.5	E-POWER lite	Remark
30	VDDAU	VDDAU	VDDAU	
31	BYP	BYP	BYP	
32	IREF	IREF	IREF	
33	VSSR	VSSR	VSSR	
34	VANA	VANA	VANA	
35	VDDA	VDDA	VDDA	
36	VRF0	VCXOEN	VCXOEN	Difference between V0.5 and V1.5
37	VRF3	VRF3	---	E-POWERlite modified
38	VRF2	VRF2	VRF2	
39	VDDRF	VDDRF	VDDRF	
40	VRF1	VRF1	VRF1	
41	INTOUT	INTOUT	INTOUT	
42	VRTC	VRTC	VRTC	
43	VDDCH	VDDCH	VDDCH	
44	VCHC	VCHC	VCHC	
45	VLBB1	VLBB1	VLBB1	
46	VDDC	VDDC	VDDC	
47	VLBB2	VLBB2	VLBB2	
48	RESETQ	RESETQ	RESETQ	
*	VSSA	VSSA	VSSA	
*	VSSD	VSSD	VSSD	
*	VSSCHP	VSSCHP	---	
*	---	VSSUSB	---	Difference between V0.5 and V1.5
*	VSSL	VSSL	VSSL	

2.3.3 Migration of Registers

Table 2-4 compares the register contents of the SM-POWER V1.5 and E-POWERlite. The register access is completely identical for the SM-POWER V1.5 and E-POWERlite with the following exceptions:

- The registers of circuits that have been removed in the E-POWERlite have no function.

CONFIDENTIAL

- The function of LRF3EN does not exist.
- For using the enhanced features of the audio amplifier register **AUDCTRL2** must be accessed.
- It is possible to distinguish by software between E-POWERlite and SM-POWER V1.5 by reading bit 0 of register **CHST**.

Table 2-4 Register Comparison between POWER Chips

Address [Hex].	Access	SM-POWER V1.5	E-POWERlite	Function inside E-POWERlite
00	W	-	-	
01	W	RESCTRL	RESCTRL	Reset control
02	W	PWCTRL1	PWCTRL1	LINT, LANA, LBB1, LBB2
03	W	PWCTRL2	PWCTRL2	SDBB
04	W	CHCTRL1	CHCTRL1	Charger control
05	W	INTCTRL1	INTCTRL1	Interrupt control
06	W	INTCTRL2	INTCTRL2	Interrupt control
07	W	PWCTRL3	PWCTRL3	LRF2
08	W	CHCTRL2	CHCTRL2	Charger control
0A	W	LEDCTRL1	LEDCTRL1	LED control
0B	W	DRVCTRL	DRVCTRL	Vibrator driver control
0C	W	USBCTRL	AUDCTRL2	Audio amplifier control
0D	W	AUDCTRL	AUDCTRL	Audio amplifier control
0E	W	PWCTRL4	PWCTRL4	LRFC, LRF1
11	W	PWCRTL5	PWCRTL5	LSIM, LSIM2
12	W	PWCTRL6	PWCTRL6	LMMC
13	W	LEDCTRL2	LEDCTRL2	LED control
80	R	GEF1	GEF1	General error flags
81	R	ISF	ISF	Interrupt source flags
82	R	CHST	CHST	Charger status
83	R	GEF2	GEF2	General error flags

3 Functional Description

3.1 Overview of Power Supply Functions

An overview of the power supply functions is given in Table 3-1. Output voltage values after start-up are printed bold.

Table 3-1 Overview of Power Supplies

Regulator		Output Voltage	Min. Output Current	Auto Startup	Supplied Device / Remark
Name	**Type**	**V**	**mA**		
SDBB	DC/DC converter	1.92 1.86 **1.80** 1.50	400	Yes	Input for LBB1, LBB2 and LRFC, supply for EBU, SDRAM I/O and others
LBB1	linear regulator	**1.50** 1.65	170	Yes	E-GOLDlite DSP (TeakLite®) supply (supplied by SDBB)
LBB2	linear regulator	**1.50** 1.65	170	Yes	E-GOLDlite core supply including C166 (supplied by SDBB)
LANA	low-noise LDO	**2.65**	220	Yes	Supply for analog part in E-GOLDlite
LINT	LDO	**2.72**	135	Yes	E-GOLDlite interface supply: I2C, SSC1-3, ETM
LSIM	LDO	**2.85** 1.80	22	Yes	E-GOLDlite SIM Interface
LSIM2	LDO	**2.85** 1.80	200	Yes	Supply for peripherals
LMMC	LDO	**2.85** 1.80	22	Yes	Supply for peripherals
LRFC	low-noise linear regulator	**1.50**	120	No	SMARTi-SD core (supplied by SDBB)
LRF1	low-noise LDO	**2.50**	120	No	SMARTi-SD main supply

Table 3-1 Overview of Power Supplies

Regulator		Output Voltage	Min. Output Current	Auto Startup	Supplied Device / Remark
Name	**Type**	**V**	**mA**		
LRF2	low-noise LDO	2.70 **2.50**	10	Yes	Supply for VCXO
LRTC	linear regulator	**2.11**	0.3	Yes	Ultra-low zero-load current

3.2 Control Inputs and Standby Behaviour

Control Input ON

ON is a power-on input for E-POWERlite with 2 active high levels (see **Figure 3-1**). It can be triggered by

- a push button
- the RTCOUT output of the E-GOLDlite

To detect if the push-button is pressed during system operation the logic level at pin ON or a level change (if bit EION in **INTCTRL2** is set to 1) is recorded in bit LON of the **ISF** register. LON is only set if the high level of the voltage at pin ON is above V_{IHdet} (see **Table 5-8 "AC/DC Characteristics of Digital Signals" on Page 64**).

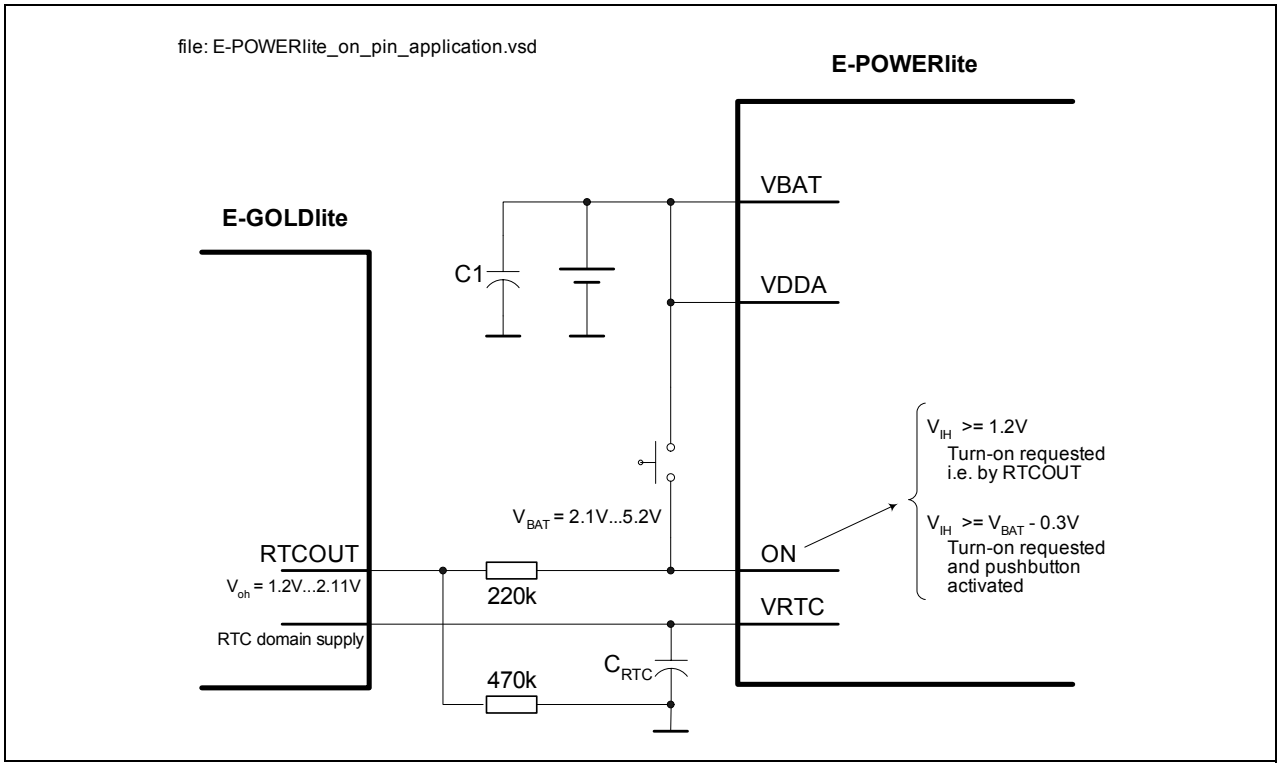

Figure 3-1 Pin ON Application Circuit

Control Input VCXOEN

VCXOEN is a control signals that allows switching the state of the power mangement functions of the PMB6814 V1.0 E-POWERlite with a single signal.

VCXOEN = 0, standby mode

VCXOEN = 1, active mode

- The regulators LBB1, LRFC, LRF1, LRF2 can be programmed to a configuration that allows to control the **on/off** state with VCXOEN.
- The regulators LINT, LSIM, LSIM2, LMMC can be programmed to a configuration that allows to control the **on/standby** state with VCXOEN.
- The SDBB regulator can be programmed to a configuration that allows to control the toggling between PWM- and power saving PFM-mode with VCXOEN.

Table 3-2shows a list of all functions that can be controlled by VCXOEN and the required register programming to allow control with VCXOEN.

Table 3-2 Control Function of VCXOEN

Regulator	Register Setting to allow Control by VCXOEN	Function of Regulator	
		VCXOEN = 0	VCXOEN = 1
LRFC	PWCTRL4 / LRFCMD = 01	off	on

Table 3-2 Control Function of VCXOEN

Regulator	Register Setting to allow Control by VCXOEN	Function of Regulator	
		VCXOEN = 0	VCXOEN = 1
LRF1	PWCTRL4 / LRF1MD = 01	off	on
LRF2	PWCTRL3 / LRF2MD = 01 PWCTRL3 / LRF2MD = 10	off	on
LBB1	PWCTRL1 / LBBMD = 01	off	on
SDBB	PWCTRL2 / SDBBMD = 01	PFM	PWM
LINT	PWCTRL1 / LINTMD = 0	standby	on
LSIM	PWCTRL5 / LSIMMD = 01	standby	on
LSIM2	PWCTRL5 / LSIM2MD = 001 PWCTRL5 / LSIM2MD = 011	standby	on
LMMC	PWCTRL6 / LMMCMD = 01	standby	on

In standby mode the dynamic performance of regulators LINT, LSIM, LSIM2 and LMMC is reduced. Please see **Table 5-12**, **Table 5-13** and **Table 5-14** for details.

3.3 Step-Down Converter for Baseband (SDBB)

The Step-Down Converter SDBB (Step-Down Baseband) converts the battery voltage to an artificial supply rail VDDC between 1.50 V and 1.92 V (programmable). VDDC provides the input current for:

- Baseband regulators LBB1 and LBB2
- External bus unit of E-GOLDlite
- I/O of an external memory IC
- LRFC regulator

Any current demand from these consumers counts against the specified output current and output current change rate of SDBB.

The SDBB can be operated in two different modes:

- PWM: for high currents
- PFM: for low currents (minimized power consumption!)

3.3.1 Automatic Switching between Modes

The PMB6814 V1.0 E-POWERlite can react automatically to increased current requirements by switching automatically from PFM mode to PWM mode.

If an overload condition occurs in PFM mode and bit ASPWM in register **PWCTRL2** is set an automatic switch-back to PWM mode will occur.

CONFIDENTIAL

To re-enable PFM mode after an automatic switch-back, first PWM mode must be enabled again by hardware. PFM mode can be enabled either by software control or by using VCXOEN as control signal. The state diagram for switching back to PFM is shown in **Figure 3-2** and **Figure 3-3** for both modes.

- **Software controlled mode:** In case of forced PFM mode the register must be reset to PWM mode before it can be programmed to forced PFM mode again. **Figure 3-2** shows the state diagram.
- **VCXOEN controlled mode:** In case of VCXOEN controlled PFM mode the next falling edge of signal VCXOEN will re-enable PFM mode. **Figure 3-3** shows the state diagram.

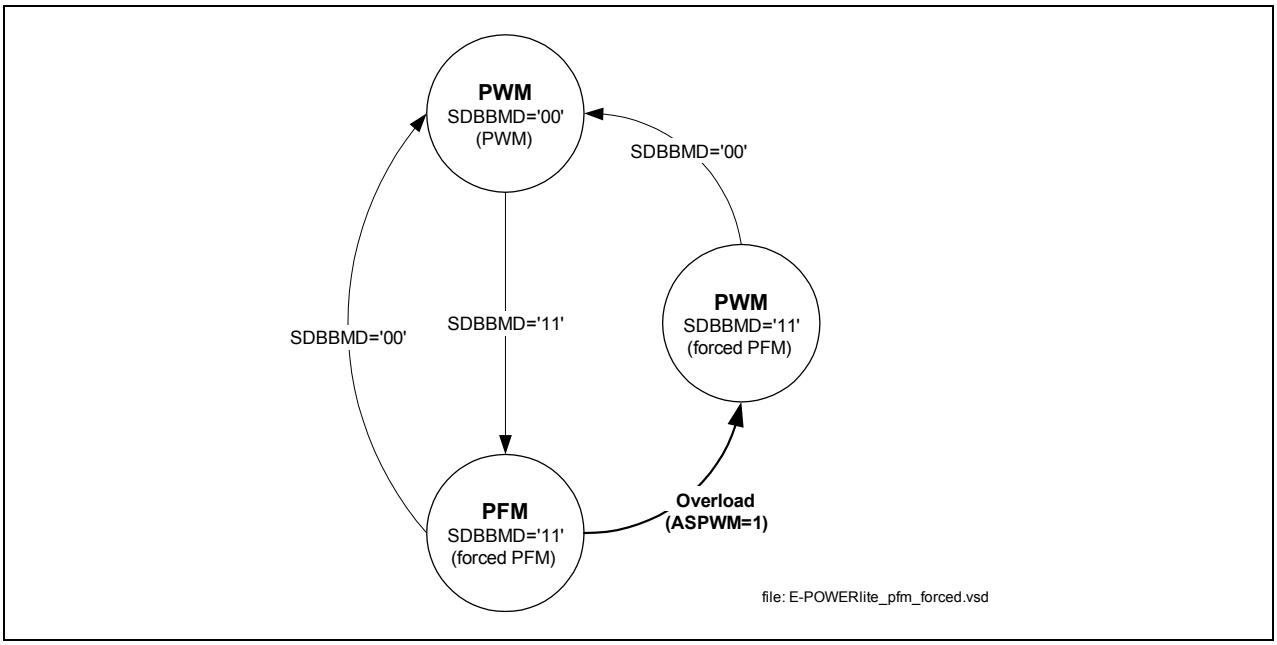

Figure 3-2 State Diagram for Switch-back from Software controlled PFM Mode

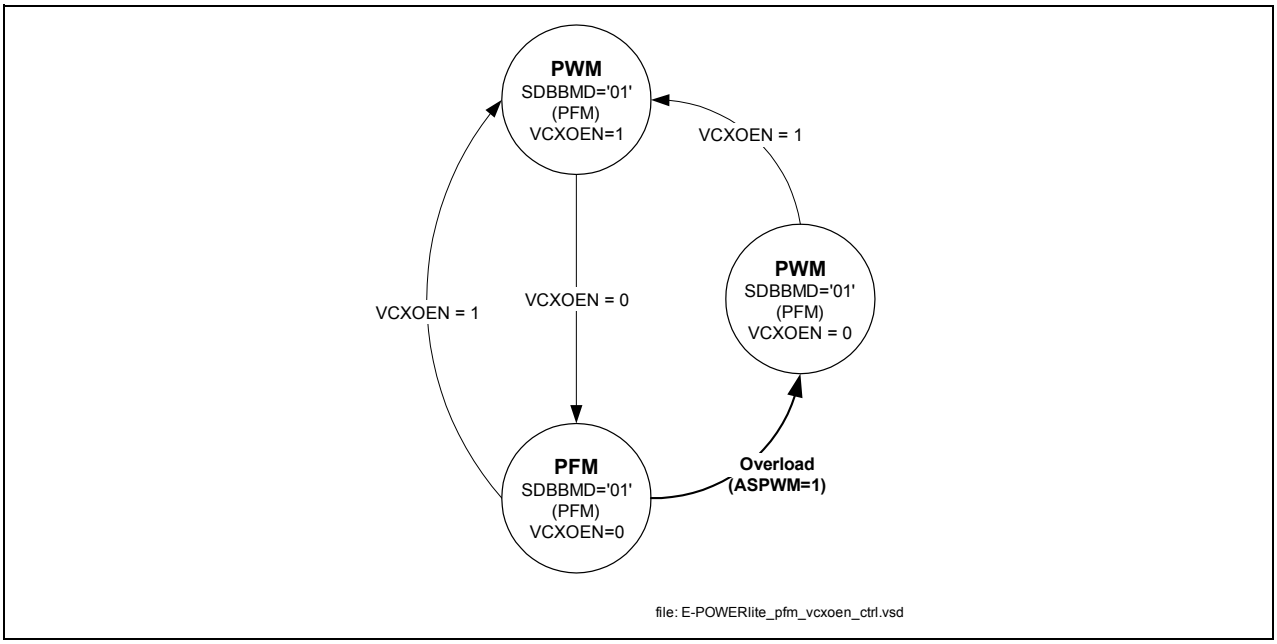

Figure 3-3 State Diagram for Switch-back from VCXOEN controlled PFM Mode

3.4 Regulator LANA

Regulator LANA is designed to supply the analog part of the E-GOLDlite. The maximum supply current permits a maximum audio output power of 2 x 20 mW on the stereo headset outputs at a load of 15 Ohms.

3.5 Audio Amplifier

The audio buffer is a fully differential unity gain amplifier for amplification of the output signal on the E-GOLDlite outputs EPp1 and EPn1. The audio amplifier is directly supplied by the battery thereby permitting maximum output power and saving silicon for the regulator. This requires a high PSRR to be able to tolerate the high ripple voltage on the battery supply during transmit bursts generated by the PA.

The audio path interface between E-GOLDlite and E-POWERlite and its typical levels are shown in **Figure 3-4**. For good performance a PCB design with a low ohmic connection between the two grounds AGND_force and VSSR is recommended.

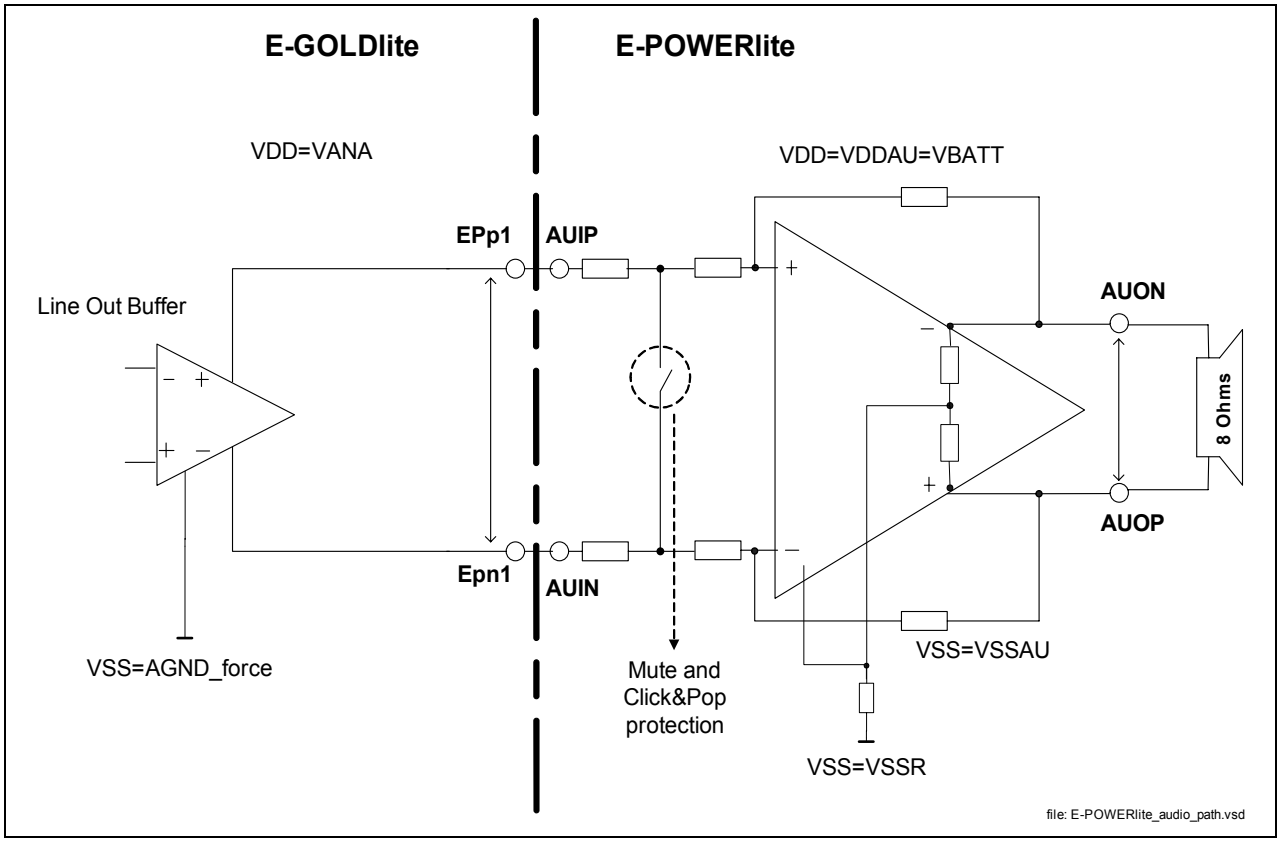

Figure 3-4 Audio Path

The startup gain of the audio amplifier is -6.0 dB. It can be switched to -1.2 dB for digital ringing, +2.7 dB (permitting an audio output power of 400 mW on an 8 Ohm load) for voice and +7.6 dB for sound ringing.

3.5.1 Power Dissipation

Care has to be taken to limit the power dissipation of the audio amplifier in accordance with the thermal dissipation of other regulators, the thermal resistance of the package and the application environment.

The temperature of the junction of the device is sensed by a temperature sense element. If a temperatur of 120 °C is exceeded the overtemperatur warning sensor is triggered. Depending on activation of bit RAGOTW in register **INTCTRL2** the gain of the audio amplifier is reduced to -6.0 dB to reduce power dissipation.

3.5.2 Click and Pop Protection

Depop circuitry to prevent noise during turn-on and turn-off transitions is included in E-POWERlite's Audio Amplifier. The general principle of a click & pop circuit is to avoid unsymmetrical input signals during startup and shutdown of the amplifier circuit. In this

phase the audio amplifier can easily go into saturation by an unsymmetrical input. This may cause a disturbing click or pop noise.

The concept used in E-POWERlite is to raise the gain in 32µs steps:

- Starting point: amplifier is powered down and outputs are pulled to ground
- The first gain setting is "mute" which shorts the input signals across a part of the amplifiere's input resistors. This prevents that an unsymmetrical signal is applied during startup of the amplifier circuit. Note that an unsymmetrical signal can also be the consequence of a DC offset in the audio path just before E-POWERlite.
- After 32 µs the next gain setting is activated, which is -6 dB. Then the next gain setting is activated until the desired gain programmed in register **AUDCTRL** is reached .

In case the target gain is 7.6 dB the startup sequence may last for approximately 4 x 32 µs = 128 µs.

Shutdown via Bit AUDON in register **AUDCTRL** is done by the following sequence:

- Activate mute function for 32 µs.
- Decreasing the gain settings in 32 µs steps.
- Activate the pull-downs of the outputs.

Shutdown can take up to approximately 128 µs depending on the initial gain.

To avoid switching noise it is recommended to apply the following turn-on and turn-off sequences for the audio path:

- Turn on audio output of E-GOLDlite prior to audio amplifier on E-POWERlite.
- Turn off audio amplifier on E-POWERlite prior to audio output of E-GOLDlite.

3.5.3 Tristate Outputs

The E-POWERlite audio amplifier outputs can be programmed to tristate mode. This allows the system to connect another audio source to the loudspeaker in parallel for alternative usage. This feature can be activated by bit TRISTATE in register **AUDCTRL**. This bit is set to 0 by default enabling output's connection to ground for muting purposes, as shown in **Figure 3-5**. Switching this bit to 1 enables tri-state output. **Figure 3-6** shows a typical timing for entering and leaving tristate mode.

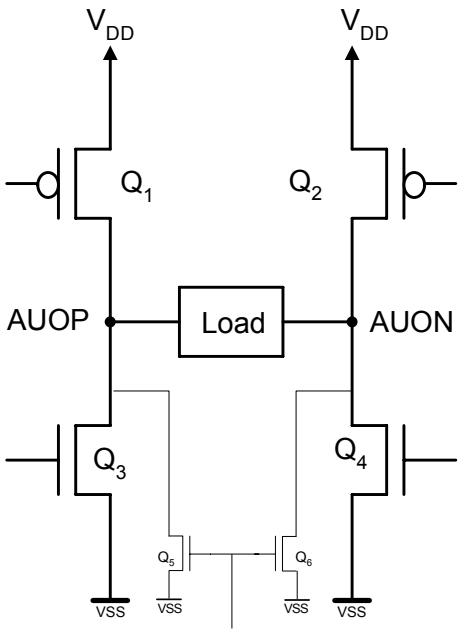

Figure 3-5 Audio Amplifier Output Stage

*Note: It is recommended to set bit TRISTATE = 0 before starting the audio amplifier in E-POWERlite in order to have a well-defined startup point (for further details see **Figure 3-6**).*

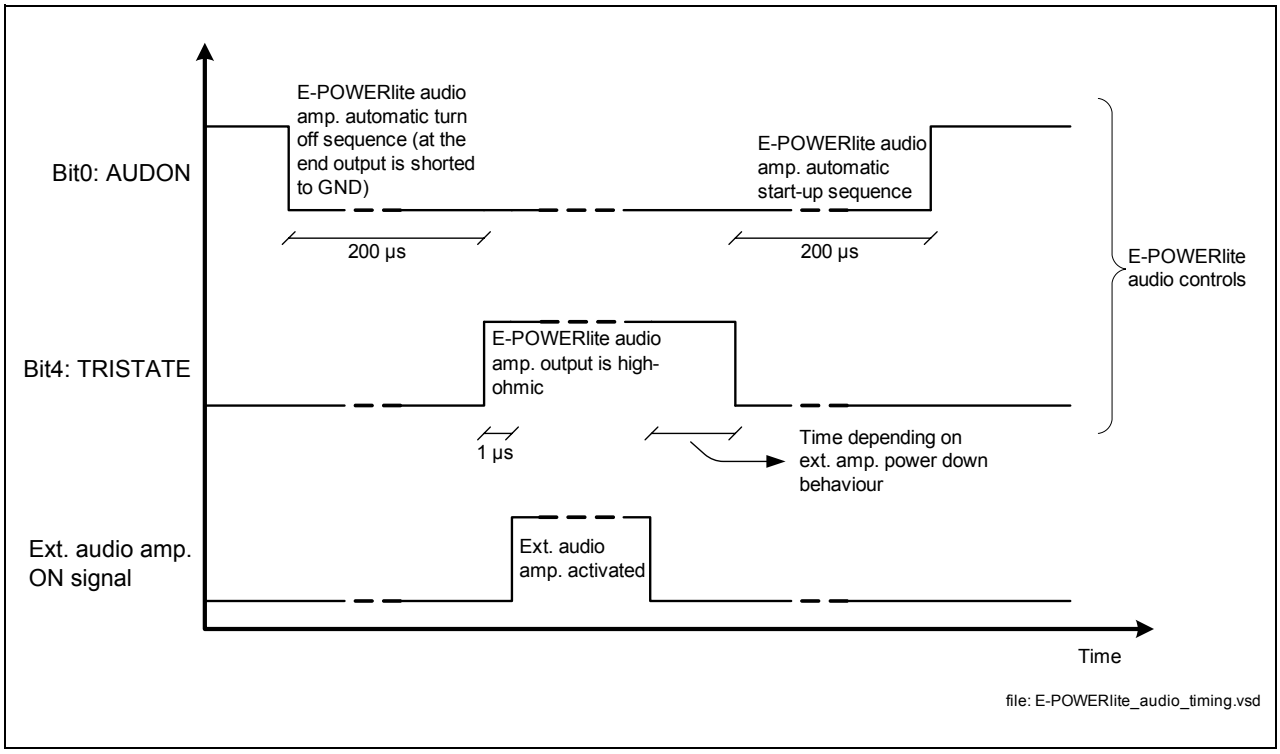

Figure 3-6 Combination of E-POWERlite internal Audio Amplifier and optional external Device: Turn-off, Tristate and Turn-on Timing Diagram

3.5.4 Protection against Short Circuits

The Audio Amplifier offers a short circuit protection by limiting the current to approx. 700mA if a short occurs between pins AUOP and AUON or AUOP/AUON and PCB ground.

Note: A short between AUOP/AUON and battery plus pole is not protected.

3.5.5 Programmable Common Mode Voltage

Per default the audio amplifier is designed for optimum performance concerning THD and power at a battery voltage of 3.3 V. To allow more output power for higher battery voltages the following programming is possible:

- The output common mode voltage of the audio amplifier can be programmed, depending on the battery voltage in register **AUDCTRL2**. It is recommendet to select the common mode voltage V_{outcm} always to half the battery voltage V_{bat}. This setup offers maximum possible output swing with lowest distortion. In this case the maximum possible output power is only limited by the battery voltage itself. In other words: Maximum possible output power depends on actual battery voltage (see **Table 5-19**).
- The gain of the audio amplifier can be programmed to maximum output swing even at limited input swing in register **AUDCTRL2** and **AUDCTRL**.

3.6 Vibrator Driver

The universal voltage source is a voltage-step programmable, switchable high side constant voltage source. The driver provides average load current limiting (see register **DRVCTRL** and **Table 5-23**). The low side of the load can be connected directly to ground.

The circuit has a built-in soft startup and shutdown function and does not need any external circuitry. If needed, a bypass filtering capacitor at the output can be added.

A short-circuit current limitation is included.

3.7 LED Drivers

The complete configuration of the E-POWERlite LED drivers is shown in **Figure 3-7**.

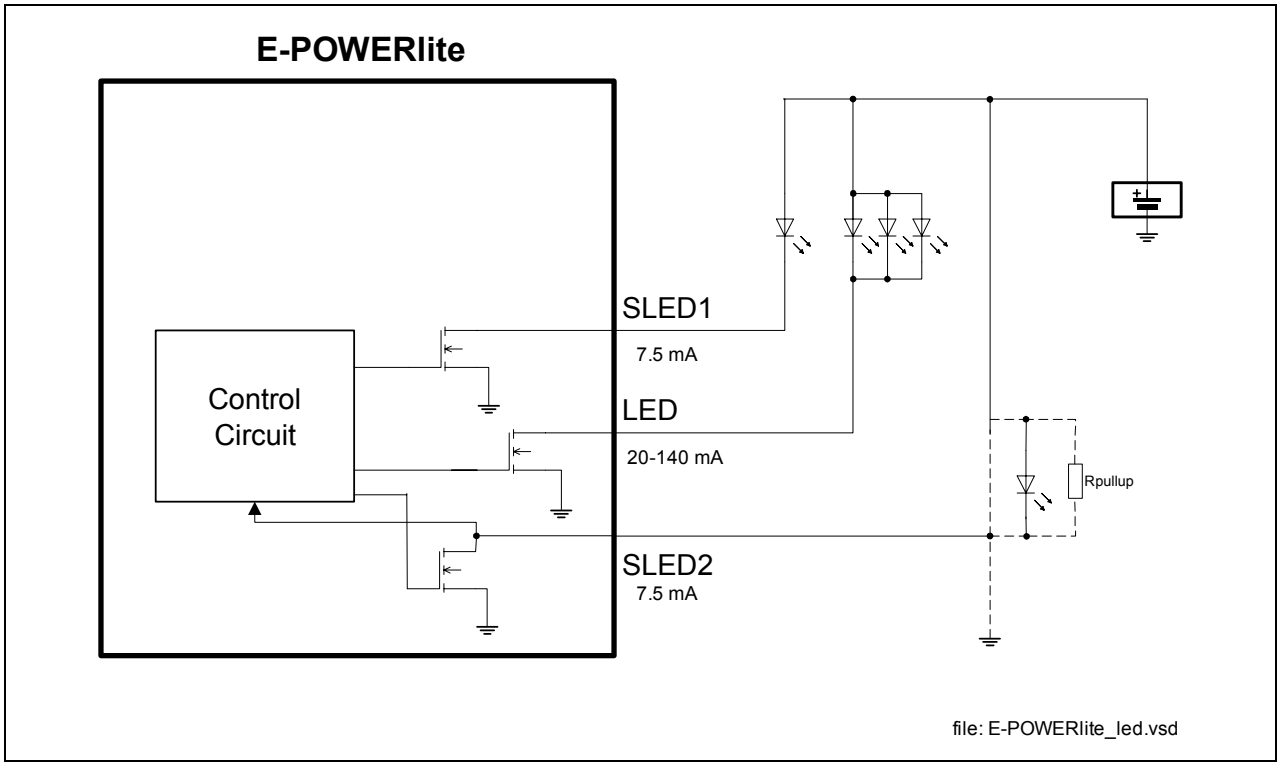

Figure 3-7 Backlight and signalling LEDs

3.7.1 Backlight LED Driver

The backlight LED driver is suitable for driving most commercially available LEDs in the red, orange, yellow and green range. The driver is a switchable low side constant current source. It is programmable in 7 steps in the range from 20 mA to 140 mA with a step width of 20 mA (see register **LEDCTRL1**). The anode of the LEDs can be attached directly to the battery.

The power dissipation of the driver has to be taken into account for calculation of the maximum junction temperature. It can be minimized by selecting appropriate resistors in series with the LEDs.

The LED driver function consists of a PWM control with a fundamental frequency of about 60 Hz generated from the internal clock frequency of 500 kHz by division by 8192. Using register **LEDCTRL1** the duty cycle of the LED current can be set in 63 steps in the range from 0.5% to 100%. By sending a sequence of appropriate commands to E-POWERlite a soft dim function can easily be implemented.

3.7.2 Signalling LED Drivers

The signalling LED drivers are switchable low side constant current sources. In normal operation they can be controlled by the bits SLED1ON and SLED2On in register **LEDCTRL2**.

3.7.3 Precharge Signalling Function

During precharge phase the open drain LED driver at pin SLED1 is always enabled, thereby signalling precharging operation to the user if a LED is connected between this pin and the battery. If no additional LED is planned, SLED1 can be shorted to GND. During precharge phase the level on SLED2 sets the value of the precharge current of 60 mA or 120 mA depending on battery voltage (for details see **Section 3.8.1**).

3.8 Charge Control Function

E-POWERlite provides together with external p-channel FETs like Infineon BSL 211SP, Siliconix Si3443 or Si3441 and an external AC-adapter a complete charge control function. The following batteries with 4.1, 4.2 or 5.2 V can be used:

- Li-Ion (1 cell)
- Li-Ion-Polymer (1 cell)
- NiMH (3 cells), E-POWERlite devices to support NiMH cells are available on request

The supported external pass devices permit charging of the battery with currents of up to $I_{ACadapt}$. The voltage between pins VDDCH and VCHC is internally limited to less than 5.5 V. Thereby external FETs with a V_{GSmax} of 5.5 V can be used, even if the external AC adapter voltage rises up to 12 V.

The application circuit for charge control is shown in **Figure 3-8**.

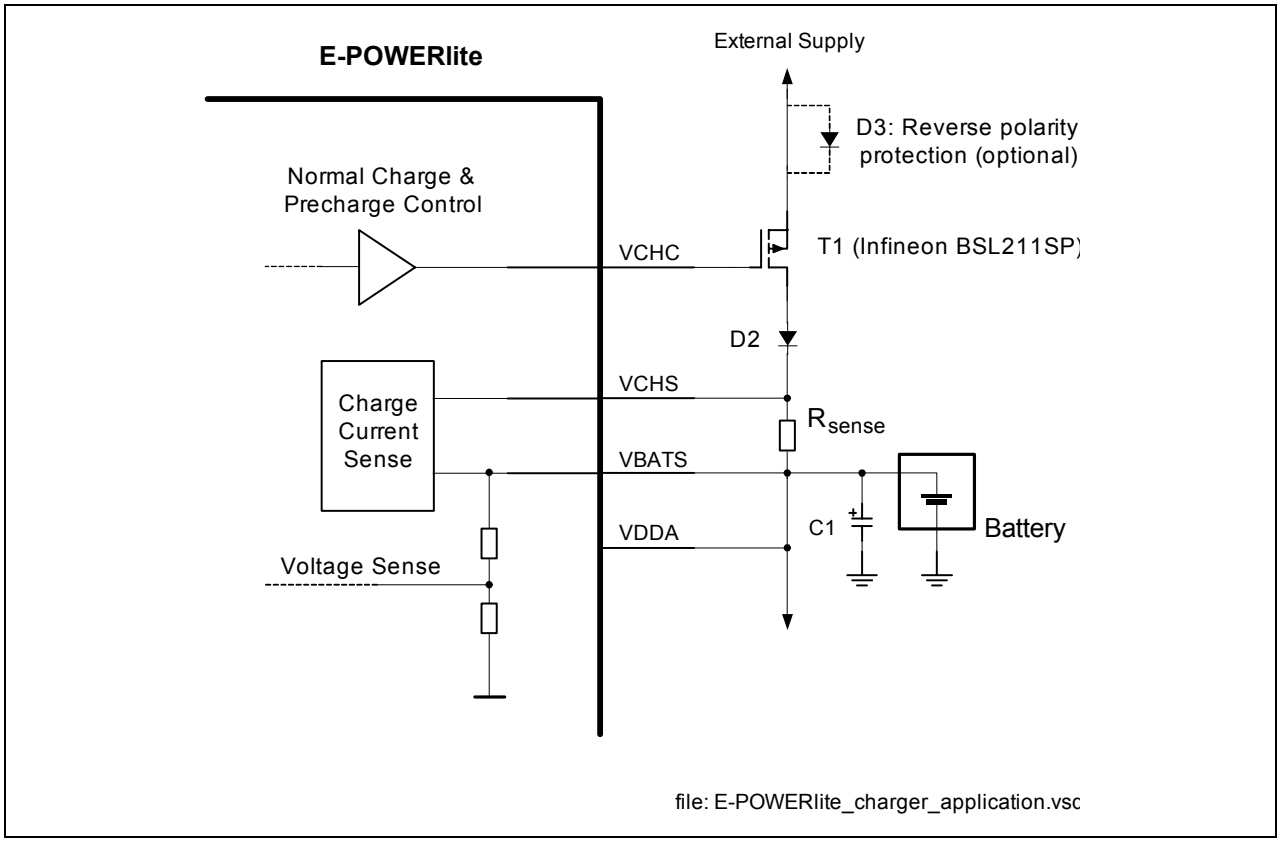

Figure 3-8 Application Circuit for Charge Control

Diode D2 is required to prevent the drain-bulk diode of FET T1 from discharging the battery when the AC adapter voltage drops below the battery voltage.

Diode D3 is optional if reverse polarity protection is required because plugs are mistakeable.

Note: In case VDDCHmin of 5 V is required please avoid diode D3 by using a mechanical reverse polarity protection because it will further reduce the headroom voltage which is available for charging.

The following charge modes are supported by E-POWERlite:

When the AC-adapter is plugged:

- Precharge function for deeply discharged batteries

When the AC adapter is plugged and battery voltage has exceeded V_{BATon}.

- Constant current charging with programmable current limitation from 400 mA to 1.1 A.
- Constant voltage charging with 3 programmable voltage limitations for Li-Ion, Li-Polymer and NiMH batteries
- Pulse charging option with selectable pulse width for top-off charging of Li-Ion batteries
- Charging current monitoring for handling the top-off charging phase of Li-Ion batteries.

3.8.1 Precharge Functionality

The precharge current function delivers a typical current of I_{Prech} (see **Table 5-24**) to the battery whenever the AC adapter is plugged. This current is used for bringing up a deeply discharged battery to a voltage level where the system can turn on again. This high amount of precharge current is necessary to ensure sufficient supply during the system startup phase when the controller usually boots its software. A proper startup is therefore possible even with deeply discharged batteries.

A selection between two precharge current values of I_{Prech1} and I_{Prech2} is possible by the logic level at pin SLED2. With deeply discharged batteries (voltages of about 1.2 V or less) only the precharge current of I_{Prech1} is allowed (see **Table**). The precharge current can be set as shown in **Figure 3-7**: if both I_{Prech1} precharge current and a signalling LED are needed. A pull-up resistor should then be put in parallel to the LED connected to pin SLED2 to avoid logic level uncertainties at this pin. Otherwise pin SLED2 can be connected directly either to ground or to the battery voltage.

Table 3-3 Precharge Current Selection

SLED1	SLED2	Precharge current
on during precharge	pin shorted to GND	I_{Prech2} (120 mA)
	pin shorted to VBAT or connected to LED's cathode	I_{Prech1} (60 mA)
	pin wherever connected, so long as battery voltage is less or equal than approximately 1.2 V	I_{Prech1} (60 mA)

As soon as the system has started, the precharge function can be turned off by setting bit PREOFF = 1 in register **CHCTRL2**.

To ensure system stability in case of battery removal a window comparator takes care that the precharger never raises the battery node of E-POWERlite to voltages above V_{PREmax} (see **Table 5-24**). If V_{PREmax} is reached the comparator will automatically turn off the precharge function.

The precharge function is turned on again as soon as the voltage goes below V_{PREmin}. This feature avoids that the voltage at the battery node gets too high no matter if there is a battery or not and it makes sure that the system does not turn on and off all the time.

3.8.2 Constant Current Charging

The constant current charging function is only available if the battery voltage is higher than V_{BATon}. In this case an external supply voltage applied to pin VDDCH higher than $V_{DDCHmin}$ will turn on E-POWERlite and as a consequence power up E-GOLDlite.

Constant current charging can be initiated by E-GOLDlite via the I^2C-bus interface by activating bit ON in the charger control register **CHCTRL1**.

The current limitation can be activated and pre-programmed by software in register **CHCTRL2**.

Note: Never program a charge current limitation which is above the internal current limitation of the AC-adapter. This may cause instability because the two current limitations could begin to fight against each other.

As soon as the sum of the internal voltage of the battery and of the voltage drop in the battery caused by the charging current exceeds the preprogrammed value V_{CHmax} the charge control circuit changes automatically to constant voltage mode. E-POWERlite can be programmed to generate an interrupt when this happens.

3.8.3 Constant Voltage Charging

To be able to charge Li-Ion batteries up to their full capacitance E-POWERlite provides a precisely programmable voltage limiting. The end voltages for the charging process can be programed to 3 different values of V_{CHmax}. The maximum charging voltage is selected by bits VMAX in register **CHCTRL1**. During voltage limitation, E-POWERlite will reduce the current through transistor T1 in any case, as soon as the voltage on the battery rises to the permitted maximum voltage. In this state the circuit operates like a linear regulator in regulation and constant current charging is replaced by constant voltage charging.

For Li-Ion batteries a constant-voltage charging of either VCHmax1 or VCHmax2 can be chosen.

Note: Never program a V_{CHmax} voltage which is above the maximum allowed voltage of the used battery type.

Note: For safety reasons, when using Li-Ion batteries we strongly recommend to use a battery pack with a safety switch including overvoltage protection.

For NiMH batteries the maximum charging voltage is limited to V_{CHmax3}. This maximum voltage is mainly required for the protection of the E-POWERlite itself.

In continuous charging mode the E-GOLDlite controller will turn on and off the charging process. In pulse charging mode only turn-on is required. Turn-off is done automatically by E-POWERlite after a preselected time.

3.8.4 Pulse Charging

Pulse charging (bit PCH = 1 in register **CHCTRL1**) is usually used for top-off charging of Li-Ion and Li-Polymer batteries, when the maximum continuous charging voltage of the Li-Ion battery (V_{CHmax1} or V_{CHmax2}) has been reached. In pulse charging mode each charging pulse has to be triggered by a command to E-POWERlite specifying the length of the charging pulse. The pulse charging mode of E-POWERlite permits generation of

a charging pulse of a predefined length without requiring the E-GOLDlite controller to turn off the charging process. This reduces the processing load on the E-GOLDlite controller and avoids the risk of generating a charge pulse of excessive length due to a software problem in the E-GOLDlite controller.

In pulse charging mode voltage limitation can be used in an alternative way. Bit CHMD in the charger status register **CHST** will always be reset to 0 when the voltage on pin VBATS reaches the preprogrammed level VCHmax . If bit VL in register **CHCTRL1** is set to 1 E-POWERlite will switch from constant current charging to constant voltage charging as in continuous charging mode. If bit VL in register **CHCTRL1** is set to 0 E-POWERlite will stop charging as soon as bit CHMD has been reset. If E-POWERlite has been set up appropriately (bit EICHMD=1 in register **INTCTRL1**) output pin INTOUT will toggle, signalling the change to the E-GOLDlite controller.

During pulse charging, Li-Ion batteries voltage limiting can reduce the efficiency of the pulses. By selecting the highest maximum charging voltage V_{CHmax3} full charging current is present during the charging pulse.

Note: When programming V_{CHmax3} the voltage across the battery may rise above the maximum continuous charging voltage of the Li-Ion battery (V_{CHmax1} or V_{CHmax2}) for a short time interval. See battery specs for allowed exceeding of the maximum voltage during pulse charge.

Compared to continuous constant voltage charging, the power dissipation in the external p-channel FET is significantly lower in pulse charging mode. Both the battery voltage during charging and after the end of the charging pulse may be used to control the charging process. These voltages are usually measured by the E-GOLDlite controller using the A/D converters in its measurement interface.

An overview of the functionality is given in **Table 3-4**.

Table 3-4 Charging Conditions and Modes

Condition						Charging Function	Voltage Limited
Battery voltage versus V_{CHMAX}	CHST	CHCTRL1					
	CHMD	PCH	Charge mode	Voltage limit VL	Pulse timer running		
$V_{BATS} < V_{CHMAX}$	1	0	cont.	X	-	on	no
		1	pulse		no	off	-
					yes	on	no
$V_{BATS} = V_{CHMAX}$	0	0	cont.		-	on	yes
		1	pulse	0	X	off	-
				1	no	off	-
					yes	on	yes

The duration of the charging pulse can be selected by the E-GOLDlite controller in the range of about 2 ms to 262 ms with a step width of a factor of 2 by setting bits PL in register **CHCTRL1**. To trigger a charging pulse E-GOLDlite must send a command to register **CHCTRL1** with bit ON set to 1 and pulse charge mode selected. This starts an internal counter that limits the duration of the charge pulse to the selected time interval. The charge pulse is always terminated when the time-out of the internal counter has been reached. If bit VL in register **CHCTRL1** is set to 0 and the maximum charging voltage is reached it is terminated prematurely and the internal timer is reset. If E-POWERlite has been set up appropriately (bit EICHMD=1 in register **INTCTRL1**) output pin INTOUT will toggle signalling the premature termination of the charge pulse to the E-GOLDlite controller.

The pulse length is derived from the internal oscillator which is also used for the step-down converter. All pulses show the same tolerance in duration as the clock frequency of this oscillator does.

A charging pulse can be terminated by software by switching back to continuous charge mode and turning off the charger.

A minimum pulse length of 512 µs (256 internal clock cycles) will be retained under all conditions and the battery voltage will be evaluated only after this time has elapsed. Thereby instabilities of the charger immediately after turn-on will not cause any unwanted side-effects.

CONFIDENTIAL

3.8.5 Charging Current Monitoring

Especially for Li-Ion batteries E-POWERlite offers a current monitoring function which can be programmed to generate interrupts when the charging current falls short of a certain level. This is useful for handling the top-off charging phase of Li-Ion batteries.

The appropriate current level for triggering an interrupt may be set by using the bits RVM in register **CHCTRL2**.

3.9 RTC Backup Battery Charging Function

The RTC supply voltage permits charging of a NiMH backup battery. This allows significantly longer backup intervals.

3.10 Power On/Off and Reset Control Logic

Under the following conditions E-POWERlite has control over the whole system:

- battery voltage is below V_{BATon}
- mobile phone is in shutdown mode

Control is well defined in any condition by a fixed state machine structure. The state diagram with all transitions and conditions is shown in **Figure 3-9**.

For example "State 7: System Programmable" means that E-POWERlite has started all the supply voltages needed to operate E-GOLDlite and peripherals and has initiated a proper reset sequence to the controller in E-GOLDlite.

The following chapters give a more detailled description.

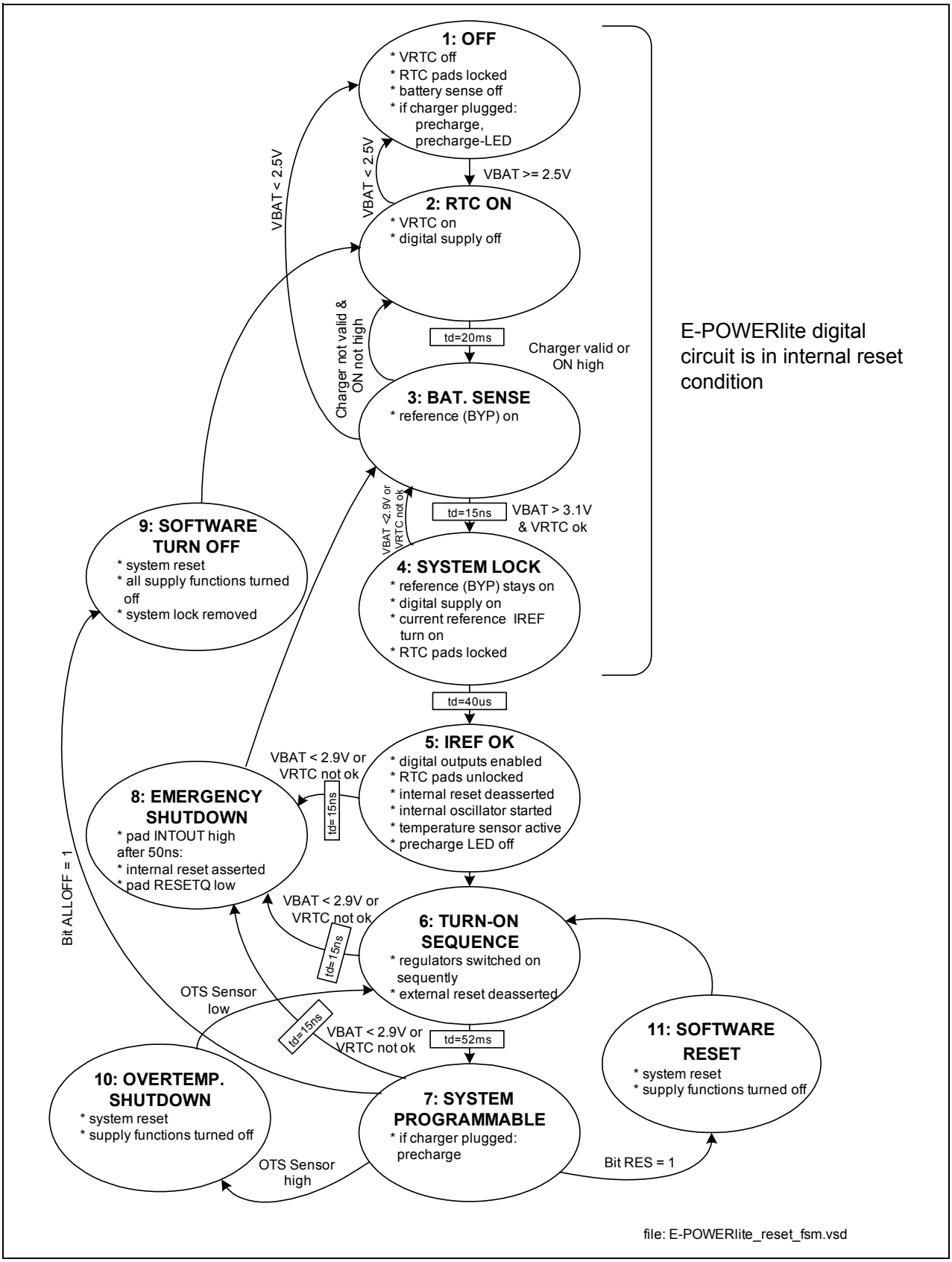

Figure 3-9 Logic States of State Machine

3.10.1 Insertion of Battery

When the battery is inserted into the handset and the battery voltage V_{BAT} rises, regulator RTC is powered up. Output pin RESETQ is tied to low level and output pin INTOUT rises to high level and locks the outputs of E-GOLDlite (OUTx) into tristate (state off). **Figure 3-10** shows this sequence.

3.10.2 Power-down Tristate Function of E-GOLDlite

The power-down tristate function isolates the outputs of E-GOLDlite from its environment whenever no proper operation of the outputs can be guaranteed. It ensures that when the battery is inserted into the handset most output pins of E-GOLDlite are locked in tristate.

This function is controlled by pins PM_INT and RESET_n of E-GOLDlite. Whenever input RESET_n of E-GOLDlite is asserted the outputs of E-GOLDlite can be put into tristate by setting input PM_INT to high level. When input PM_INT is at low level the outputs will show the reset values (if E-GOLDlite is powered up).

This function of E-GOLDlite is controlled by E-POWERlite via output pins INTOUT and RESETQ which have to be connected to pins PM_INT and RESET_n of E-GOLDlite respectively. A complete description with respect to the outputs of E-POWERlite is given in **Table 3-5**.

When E-GOLDlite is turned on, the output pins are enabled only after the core has reached its reset state. On turn-off the output pins are set to tristate prior to power-down. The outputs will remain in this state till power-up.

Table 3-5 Power-down Output Tristate Control

RESETQ	INTOUT		E-GOLDlite Outputs State
	Function	Value	
0	Output tristate control	0	Enabled
		1	Disabled
1	Interrupt	X	Enabled

The detailled timing of supply voltages and control signals is described in the following sections.

3.10.3 Turn-On

When E-POWERlite is in "State 2" and an on-condition appears (e.g. level on input ON is pulled to high level) the internal voltage reference (pin BYP) will start in order to determine if the battery voltage is sufficiently high to turn on the whole system. If yes E-POWERlite will reach "State 4" where the startup is continued without applying the start

condition any longer. The current reference (pin IREF) settles and the internal clock (about 500 kHz) and the reset counter start running.

The power-up sequence within "State 6" as listed below is controlled by the reset counter. The turn-on timing is shown in **Figure 3-10**.

1. The output voltages of several regulators (e.g. LRF2, SDBB, LINT) are started in intervalls shown in **Table 3-6** in order to avoid a surge and therefore a voltage drop on the battery during startup.
2. After the output voltages of all regulators necessary for system start-up have reached their specified value, the status RESETQ = low and INTOUT = high is kept asserted for 512 internal clock cycles (t_1 = approx. 1 ms).
3. After that time output INTOUT is set to low to enable the outputs of E-GOLDlite.
4. After another 32 x 512 reset counter clock cycles (t_2 = approx. 33 ms) output RESETQ goes high.

See **Table** for overall reset length t_{res} on RESETQ while VRF2 is running and min-max timings.

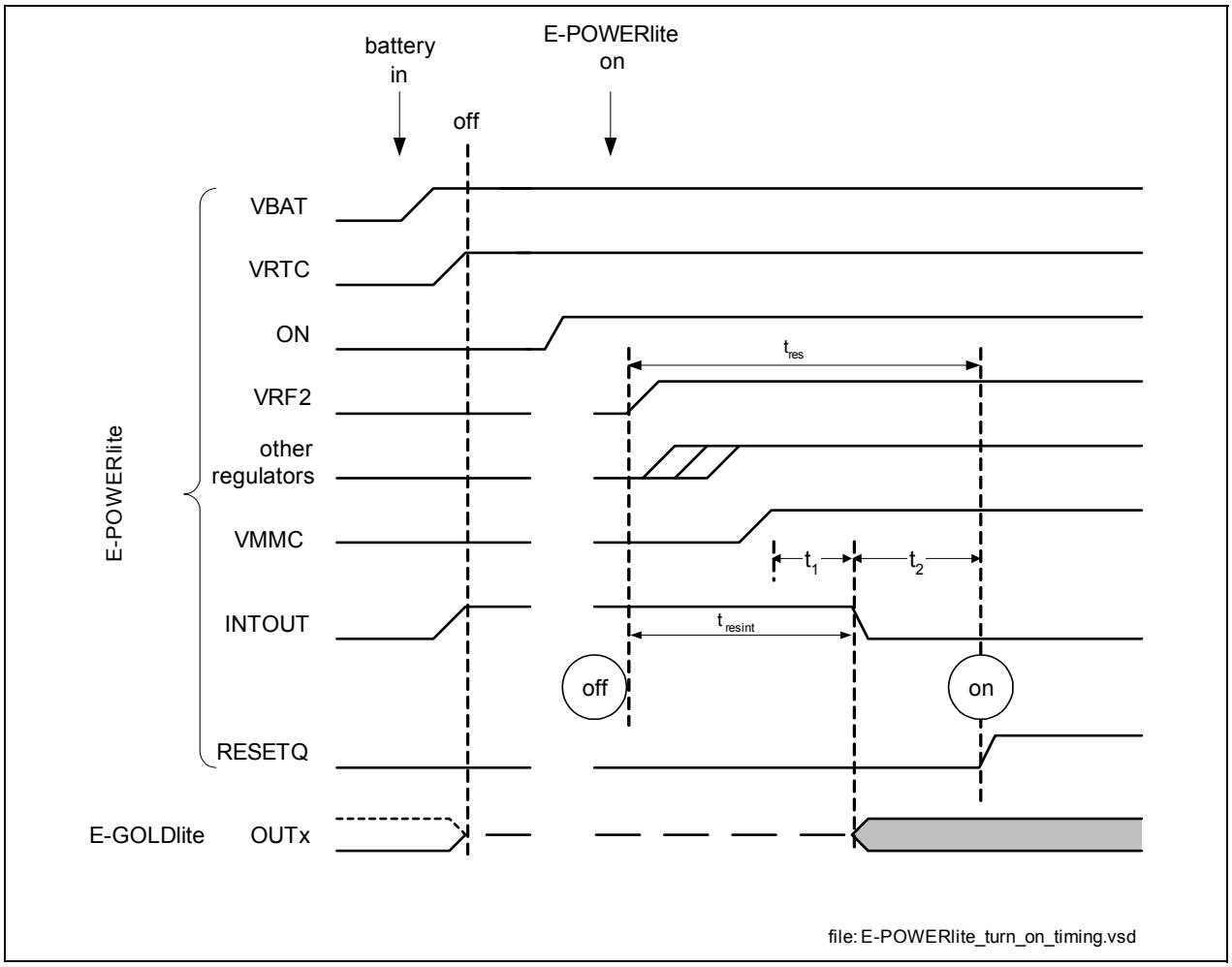

Figure 3-10 Turn-on Timing

3.10.4 Power-up Sequence

In case that the power-down tristate function as implemented in E-GOLDlite is used the power-up sequence is of minor concern since the outputs of E-GOLDlite are set to tristate as long as the system is not yet in reset state during power-up. In case no power-down tristate function is available the power-up sequence has to be kept in mind to prevent malfunction of the baseband device.

In any system the regulators should not be turned on simultaneously due to the high drain on the battery which can cause the battery voltage to drop below the operating threshold. Therefore a well defined sequence is preferable.

It is desirable to hold the core of the baseband device in reset state before enabling the I/Os. This avoids uncontrollable output signals during power-on. Inside E-GOLDlite the RESET_n pad is part of the RTC supply domain which is always powered up. This allows to power up the baseband regulators and wait for the core to reach reset state before powering up the I/O supply regulators.

The complete Power-up sequence including the delays between the steps is shown in **Table 3-6**. Delay after sequence 2 is depending on a RC-constant, but after sequence 3, the reset counter starts operation (accuracy approx. +/- 20%). The sequence has mainly been chosen to remain compatible with E-Power and E-GOLD+. All regulators not listed in **Table 3-6** have to be turned on by software afterwards.

Table shows details for timing.

Table 3-6 Turn-on Sequence of Power Supply Functions

Sequence	Function	Pin	Typical Time for Activation of next Sequence Step
			[ms]
1	LRTC INTOUT => high RESETQ => low	VRTC INTOUT RESETQ	0
2	BGREF	BYP	20
3	IREF (Reset counter started)	IREF	1
4	LRF2	VRF2	2
5	SDBB	VDDC	0
6	LBB2	VBB2	4
7	LBB1	VBB1	0
8	LINT	VINT	2

CONFIDENTIAL

Table 3-6 Turn-on Sequence of Power Supply Functions

Sequence	Function	Pin	Typical Time for Activation of next Sequence Step
			[ms]
9	LANA	VANA	2
10	LSIM	VSIM1	2
11	LSIM2	VSIM2	2
12	LMMC	VMMC	3 (ensures t_1)
13	INTOUT => low Internal reset sequence t_{resint} finished	INTOUT	33 (ensures t_2)
14	RESETQ => high	RESETQ	

3.10.5 Turn-off

Turn-off is triggered by setting the ALLOFF bit in register **RESCTRL** or by an overtemperature shut-down. After a turn-off event has been triggered the signal INTOUT is pulled to high level before the supply voltages are turned off.

Output RESETQ can be handled in two different ways in the turn-off phase :

- Bit RESDN in register **RESCTRL** is activated:
  - RESETQ is set low (reset levels are driven on the outputs of E-GOLDlite)
  - After one reset counter cycle (approx. 2 µs) INTOUT is set high (outputs of E-GOLDlite are set to tristate.
  - After one reset counter cycle (approx. 2 µs) all power supplies except LRTC are turned off.
- Bit RESDN in register **RESCTRL** is deactivated:
  - INTOUT is set high
  - After one reset counter cycle (approx. 2 µs) RESETQ is set low (outputs of E-GOLDlite are set to tristate)
  - After one reset counter cycle (approx. 2 µs) all power supplies except LRTC are turned off. All outputs of E-GOLDlite will retain their last state until they are set to tristate. Their levels have to be set appropriately by software. The normal interrupt input function of the E-GOLDlite PM_INT interrupt should be disabled prior to using this function to avoid triggering interrupt handling by the assertion of output INTOUT.

The two different ways to turn-off E-GOLDlite are shown in a state diagram in **Figure 3-12**. A description of the states is given in **Table 3-7**.

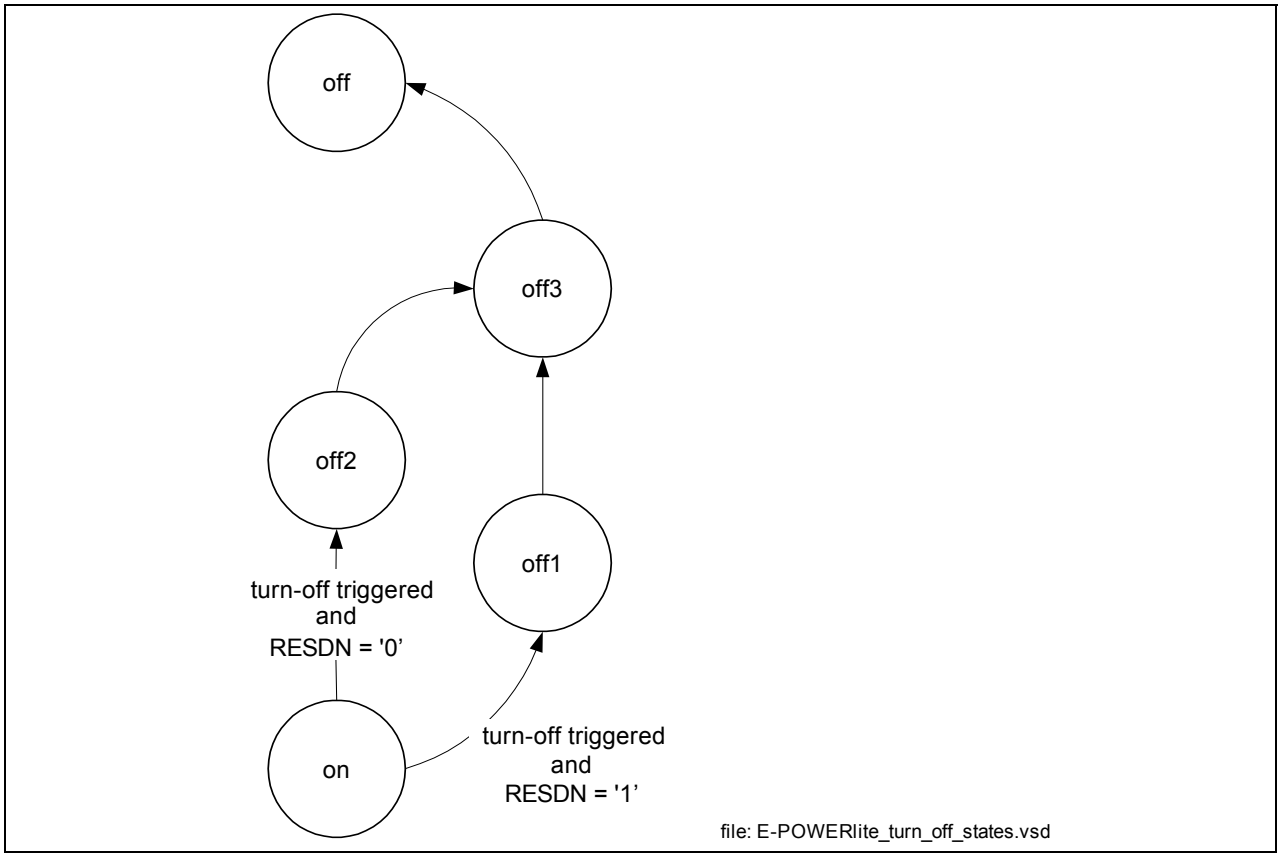

Figure 3-11 Turn-off State Diagram

Table 3-7 Turn-off State Description

State	Regulators	RESETQ	INTOUT	E-GOLDlite Outputs
on	On	H	X[1)]	active
off1	On	L	L	reset
off2		H	H	active
off3		L		tristate
off	Off	L	H	tristate

1) normal function of output INTOUT

The timing for a turn-off sequence with bit RESDN = 0 in register **RESCTRL** is shown in **Figure 3-11**.

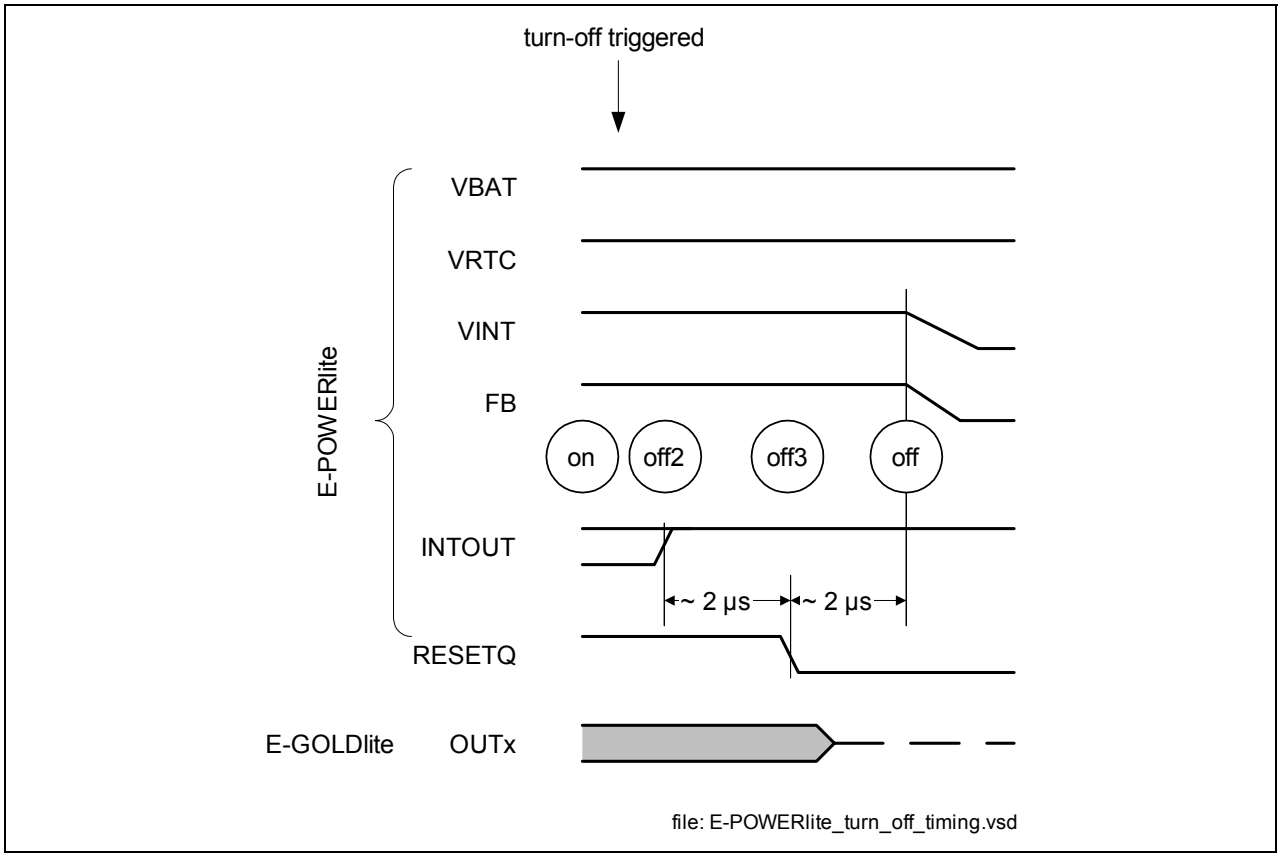

Figure 3-12 Turn-off Timing for E-GOLDlite

3.10.6 Undervoltage Shutdown

The normal way to shut down the system is triggered by the controller which senses the battery voltage and decides to turn off if the limit of operation is reached.

If the battery is pulled out or looses contact during full operation the capacitor in parallel to the battery which helps to avoid battery contact bouncing will be discharged in a couple of microseconds. The time for discharge depends on capacitor size, voltage level of the battery, consumers turned on etc.

In some cases the controller does not have sufficient time to program a shutdown. In this case E-POWERlite executes an undervoltage shutdown to the system because the undervoltage shutdown level is crossed (see **Table**).

The undervoltage shutdown immediately pulls pin INTOUT to high. Approximately 50 ns later, the internal reset of E-POWERlite is triggered and RESETQ is pulled to low. This forces the E-GOLDlite outputs to tristate.

The timing looks similar the one shown in **Figure 3-12**. The time from off2 to off3 is reduced to approximately 50 ns and the time from off3 to off is reduced to 0 ns.

Note: In undervoltage shutdown it is not possible to have a turn-off timing depending on RESDN in register **RESCTRL**.

CONFIDENTIAL

3.11 I²C-Bus Interface

3.11.1 Device Address

The I²C-bus slave interface of E-POWERlite has the following 7-bit device address.

A6	A5	A4	A3	A2	A1	A0	R/W
0	0	0	1	0	0	0	

The least signifcant bit (LSB) distinguishes between write and read operations.

The device will not react to a general call address.

The structure of all permitted I²C-bus transactions, command write with and without confirm, status read and continued read are shown in **Figure 3-13**.

It is recommended to use the output voltage on pin VINT as the VDD rail for the E-GOLDlite I²C-bus interface. To this rail the pull-up resistors will have to be connected.

If the I²C-bus interface is not used both pins SDA and SCL have to be tied to high level. In this case the reset configuration of E-POWERlite is used with all power supplies switched on and no audio, driver and charger function available except precharge.

3.11.2 Command Write

A command word consists of the device address followed by a control register address followed by a control byte. If the command has been transferred correctly the contents of the addressed control register is replaced by the contents of the control byte.

To ensure a correct transfer of command words even under adverse environmental conditions an 8-bit cyclic redundancy check (CRC) byte has to be sent immediately after the command word. The CRC has to be calculated from all transmitted bytes starting with the slave address according to the polynomial

$$C(x) = x^8 + x^2 + x^1 + 1.$$

For the calculation of the polynomial the 7-bit slave address is extended to 8 bits by adding 0 as LSB, i.e. 0x10 has to be used.

E-POWERlite will use the same polynomial to verify the correct transmission of the command. Only if the command has been positively verified the control byte will be transferred to the appropriate control register selected by the sub address and an acknowledge is given after the CRC byte to E-GOLDlite. Else the CRC byte will not be acknowledged.

If an invalid control register address is received by E-POWERlite no acknowledge will be given for the control register address byte.

*Note: Make sure never to write to any other command register addresses than those documented in **Section 4.1**. There are other registers reserved for test purposes which may cause severe side effects if their value is modified.*

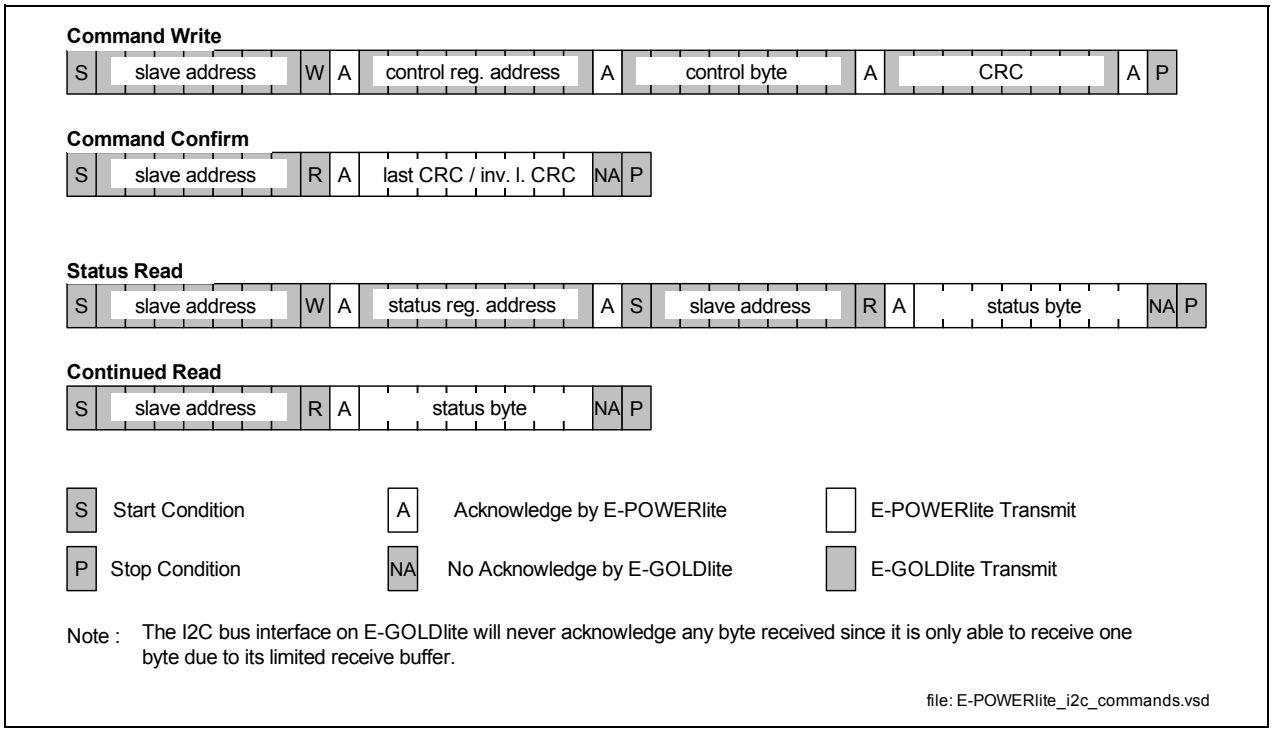

Figure 3-13 I²C-bus Interface Command Format

3.11.3 Command Confirmation

For critical commands (e.g. commands to the charger) the acknowledge bit returned by E-POWERlite may be corrupted and signal an acceptance of the command which has not been accepted due to transmission errors. To avoid this E-GOLDlite can get a command confirmation by immediately reading one byte from the E-POWERlite I²C-bus interface after the CRC byte has been transferred as shown in **Figure 3-13**. The contents of this byte will be identical to the CRC sent with the previous command if the command has been accepted and executed. If E-POWERlite detects errors in the CRC the returned byte will have all received (CRC) bits inverted. E-GOLDlite will then usually repeat the command.

3.11.4 Status Read

Register addresses starting at 80h are reserved for reading status information from E-POWERlite. After a write operation to one of these adresses the requested status information may be read with the next byte as shown in **Figure 3-13**.

In many cases repeated reading and comparison of the received status bytes can increase the reliability of the status information under adverse environmental conditions.

CONFIDENTIAL

For repeated reading the complete status read command as shown in **Figure 3-13** will have to be repeated.

This is not applicable to all register bits in all cases since some bits show the cause of the interrupt at the first read operation after the interrupt occured but show the status of the interrupt source for all consecutive readings. In this case only the reliability of the status of the interrupt source can be increased by repeated reading since the information of the cause of the interrupt is lost after the first read operation.

3.11.5 Continued Read

E-POWERlite offers a special feature to have quick access to all the status bytes. Reading of the first byte is identical to a normal status read command. Each following read operation with one byte being read at a time (continued read) will deliver the contents of the following byte (see **Figure 3-13**).

*Note: Please make sure to stop at the last status register (see **Section 4.2**).*

3.12 Software-triggered System Reset

Besides the power-on reset a reset can be triggered by setting bit RES in register **RESCTRL**. Output RESETQ will be asserted and pin INTOUT will be pulled to active level in the same way as with a power-on reset.

This function permits the system controller to trigger a system reset that resets not only the baseband device itself but also other devices (i.e.. flash devices) which might be stuck in an unrecoverable state. Such a state can occur i.e. after a software failure triggering a watchdog timer reset on the baseband device.

Bit RES will be reset by the E-POWERlite hardware after the reset time interval t_{res} has elapsed. Only after that time bit RES can be set another time.

3.13 Error Flags, Debug Mode and Interrupts

To allow the software insight to the status of the regulators, voltage and temperature sensors, the status of these devices is represented by status bits. The status bits show different behaviours to represent the status depending on the device. In general the occurence of an event or error is indicated by setting the corresponding bit to 1.

3.13.1 Error Flags

Error flags are used to show that regulators are overloaded and therefore out of regulation. These flags can be read in registers **GEF1** and **GEF2**. As long as bit DEBUG in register **INTCTRL2** is set to 0, the flags represent the current status of the modules.

3.13.2 Debug Mode

The debug mode is a helpful feature for software development. Setting bit DEBUG in register **INTCTRL2** to 1 activates a capturing mechanism in registers **GEF1** and **GEF2**. When a bit change takes place this event is stored by freezing the flag. If software is under long time test with activated debug mode, all overload conditions of regulators and also a thermal warning will be captured. After reading the registers the flag bits are updated to there current value.

3.13.3 Interrupts

Some functions and sensors of E-POWERlite can generate interrupts for E-GOLDlite.

Their status bits are represented in register **ISF** and **CHST**. When one of these status bits changes its value an interrupt request can be generated to E-GOLDlite by a rising or falling edge on pin INTOUT. The active level of an interrupt request on pin INTOUT can be determined via bit INTMD in register **INTCTRL1**.

If a change at one of these status bits shall cause an interrupt or not can be determined in register **INTCTRL1** and **INTCTRL2**. There, interrupt requests linked to status bits can be activated. If a link is activated an interrupt is triggered when an event changes the status bit. Moreover, the status bit is frozen in order to give E-GOLDlite the opportunity to find the source of the interrupt by checking bit differences in register **ISF** and **CHST** after an interrupt request had been signalled.

By performing a read command on **ISF** and **CHST** the status bit is released and represents the most recent value of its function or sensor. If this most recent value is not identical to the value that was frozen before this indicates another interrupt.

If the interrupt channel was not activated before the event took place the appropriate bit in register **ISF** or **CHST** just represents the actual status of the sensor or function without capturing anything and without signalling an interrupt request. The behaviour in this case is similar to the behaviour of Error Flags described in **Section 3.13.1**

3.14 Overtemperature Warning

If the junction temperature exceeds a temperature T_{jwarn} (see **Table "" on Page 63**) bit OTW in register **ISF** and bit OTWD in register **GEF2** are set to 1. When the junction temperature drops again below T_{jwarn} bit OTW and bit OTWD are set back to 0.

If bit EIOTW in register **INTCTRL2** is set to 1, the occurance of an overtemperature warning will set bit OTW to 1 and freeze it for debug purposes. Reading register **ISF** releases the lock and updates the status of OTW.

If bit DEBUG in register **INTCTRL2** is set to 1, the occurance of an overtemperature warning will set bit OTWD to 1 and freeze it for debug purposes. Reading register **GEF2** releases the lock and updates the status of OTWD.

CONFIDENTIAL

The reason for having two bits (OTW and OTWD) is that during software testrun an overtemperature warning can be detected without interrupting the software of the controller by an interrupt or by automatically shutting down the system.

If bit RAGOTW in register **INTCTRL2** is set to 1, the gain of the audio amplifier is reduced to -6.0 dB while bit OTW and bit OTWD are 1.

Note: It is very helpful to use the overtemperature warning bit OTWD during system development to trace thermal overloads.

3.15 Overtemperature Shutdown

If the junction temperature exceedes T_{joff} a thermal protection circuit triggers the following actions:

- Switches off all regulators except LRTC
- Switch off all charging functions
- Switch off all driver functions
- Switch off audio buffer
- Set pin RESETQ => low
- Set Bit OTS in register **ISF** is set to 1.

As soon as the temperature has fallen below T_{joff} - ΔT_{joff} E-POWERlite jumps into step 4 of the turn-on sequence described in **Table 3-6**. This causes a restart of the system.

The cause of the restart may then be verified by the E-GOLDlite by reading the contents of the Interrupt Source Flag Register **ISF**. If bit OTS is 1 after a restart an overtemperature shutdown took place.

The overtemperature shutdown function can be disabled by settting Bit OTSEN in register **INTCTRL2** to 0.

CONFIDENTIAL

4 Register Description

4.1 Control Registers

All control registers are accessable for write access only. Please note that all bits noted as reserved must not be modified with respect to their default value.

RESCTRL
RESET Control Register **(01_H)** **Reset Value: 10000000_B**

7	6	5	4	3	2	1	0
RESDN	**ALLOFF**	**reserved**					**RES**

Field	Bits	Type	Description
RESDN	7	w	**Reset in power down (see Chapter 3.10)** 0 No external reset generated on power-down 1 External reset generated on power down
ALLOFF	6	w	0 Regulator LINT on, all other regulators controlled by their individual control bits (except LRTC) 1 E-POWERlite shut down completely (except LRTC) - overrides other bits of the register
reserved	5:1	w	Reserved
RES	0	w	0 Default value after internal reset 1 Generates internal (+ external) reset

Note: In E-Power this register (address) had been used for watchdog timer control (WDCTRL). The only control bit now available has been assigned compatible to previous assignment of watchdog timer control bits permitting later enhancements for a watchdog timer.

PWCTRL1
Power Control Register 1 **(02_H)** **Reset Value: 00010111_B**

7	6	5	4	3	2	1	0
reserved			**LINTMD**	**reserved**	**LBBMD**		**LANAMD**

CONFIDENTIAL

Field	Bits	Type	Description
reserved	7:5	w	Reserved
LINTMD	4	w	0 Standby if VCXOEN=0 1 LINT on
LBBV	3	w	0 Voltage of LBB regulators at 1.5 V 1 Voltage of LBB regulators at 1.65 V
LBBMD	2:1	w	**Control mode for LBB1, LBB2** 11 LBB1 on, LBB2 on 10 LBB1 off, LBB2 on 01 LBB1 on when VCXOEN = 1, LBB2 on 00 LBB1 off, LBB2 off
LANAMD	0	w	1 LANA on 0 LANA off

PWCTRL2
Power Control Register 2 **(03_H)** **Reset Value: 00000001_B**

7	6	5	4	3	2	1	0
SDBBMD		**ASPWM**	**LPEN**	**reserved**		**VSEL**	

Field	Bits	Type	Description
SDBBMD	7:6	w	**Control mode for SDBB** 00 forced PWM mode, required for E-GOLDlite power-up phase 01 switch to PFM mode if pin VCXOEN = 0, else PWM mode 10 reserved test mode 11 forced PFM mode
ASPWM	5	w	1 automatic switchback to PWM mode enabled 0 automatic switchback to PWM mode disabled
LPEN	4	w	Internal oscillator switches off when SDBB is in PFM mode and low power mode is enabled 1 Low power mode enabled 0 Low power mode disabled
reserved	3:2	w	Reserved

CONFIDENTIAL

Field	Bits	Type	Description
VSEL	1:0	w	**SDBB output voltage selection** 00 VDDC = 1.5 V 01 VDDC = 1.8 V 10 Reserved test mode 11 VDDC = 1.92 V

PWCTRL3
Power Control Register 3 **(07_H)** **Reset Value: 00000111_B**

7	6	5	4	3	2	1	0
reserved					LRF2V	LRF2MD	

Field	Bits	Type	Description
reserved	7:3	w	Reserved
LRF2V	2	w	**Output voltage for LRF2** 0 LRF2 voltage = 2.7 V 1 LRF2 voltage = 2.5 V
LRF2MD	1:0	w	**Control mode for LRF2** 00 LRF2 off 01 LRF2 on when VCXOEN = 1 10 LRF2 off 11 LRF2 on

PWCTRL4
Power Control Register 4 **($0E_H$)** **Reset Value: 00110000_B**

7	6	5	4	3	2	1	0
LRFCMD		reserved		LRF1MD		reserved	

Field	Bits	Type	Description
LRFCMD	7:6	w	**Control mode for LRFC** 00 LRFC off 01 LRFC on when VCXOEN = 1 10 LRFC off 11 LRFC on
reserved	5:4	w	Reserved
LRF1MD	3:2	w	**Control mode for LRF1** 00 LRF1 off 01 LRF1on when VCXOEN = 1 10 LRF1 off 11 LRF1 on
reserved	1:0	w	Reserved

PWCTRL5
Power Control Register 5 **(11_H)** **Reset Value: 00111011_B**

7	6	5	4	3	2	1	0
reserved	**LSIM2V**	**LSIM2MD**			**LSIMV**	**LSIMMD**	

Field	Bits	Type	Description
reserved	7	w	Reserved
LSIM2V	6	w	**Output voltage for LSIM2** 0 LSIM2 voltage set to 2.85 V 1 LSIM2 voltage set to 1.8 V
LSIM2MD	5:3	w	**Control mode for LSIM2** 000 LSIM2 off 001 Standby if VCXOEN = 0 010 LSIM2 on 011 Standby if VCXOEN = 0 100 Standby 101 LSIM2 on 110 LSIM2 off 111 LSIM2 on
LSIMV	2	w	**Output voltage for LSIM** 0 LSIM voltage set to 2.85 V 1 LSIM voltage set to 1.8 V

CONFIDENTIAL

Field	Bits	Type	Description
LSIMMD	1:0	w	**Control mode for LSIM** 00 LSIM off 01 Standby if VCXOEN = 0 10 Standby 11 LSIM on

PWCTRL6
Power Control Register 5 **(12_H)** **Reset Value: 00000111_B**

7	6	5	4	3	2	1	0
reserved					LMMCV	LMMCMD	

Field	Bits	Type	Description
reserved	7:3	w	Reserved
LMMCV	2	w	**Output voltage for LMMC** 0 LSIM2 voltage set to 1.8 V 1 LSIM2 voltage set to 2.85 V
LMMCMD	1:0	w	**Control mode for LMMC** 00 LMMC off 01 Standby if VCXOEN = 0 10 Standby 11 LMMC on

CHCTRL1
Charger Control Register 1 **(04_H)** **Reset Value: 01000000_B**

7	6	5	4	3	2	1	0
ON	PCH	VMAX		VL	PL		

Field	Bits	Type	Description
ON	7	w	0 Charger off 1 Charger on

CONFIDENTIAL

Field	Bits	Type	Description
PCH	6	w	**Charge mode** 0 Continuous 1 Pulse
VMAX	5:4	w	**Maximum charging voltage** 00 V_{CHmax1} 01 V_{CHmax2} 10 Reserved 11 V_{CHmax3}
VL	3	w	**Voltage limit handling in pulse charge mode** 0 Shut down 1 Voltage limit
PL	2:0	w	**Charging pulse length** 000 2.048 ms (1024 clock cycles) 001 4.096 ms (2048 clock cycles) 010 8.192 ms (4096 clock cycles) 011 16.4 ms (8 k clock cycles) 100 32.8 ms (16 k clock cycles) 101 65.5 ms (32 k clock cycles) 110 131 ms (64 k clock cycles) 111 262 ms (128 k clock cycles)

CHCTRL2
Charger Control Register 2 **(08_H)** **Reset Value: 00000000_B**

7	6	5	4	3	2	1	0
RVM			**PREOFF**	**reserved**	**CHCLIM**		

CONFIDENTIAL

Field	Bits	Type	Description
RVM	7:5	w	**Reference voltage multiplier** **Level for charging current measurement (see Chapter 3.8.5)** 000 0mA 001 100mA 010 200mA 011 300mA 100 400mA 101 500mA 110 600mA 111 700mA
PREOFF	4	w	0 Precharging on 1 Precharging off
reserved	3	w	Reserved
CHCLIM	2:0	w	**Battery charge current limit** 000 400 mA 001 500 mA 010 600 mA 011 700 mA 100 800 mA 101 900 mA 110 1000 mA 111 1100 mA

INTCTRL1
Interrupt Control Register 1 **(05_H)** **Reset Value: 11101111_B**

7	6	5	4	3	2	1	0
EICHV	**EICHMD**	**EICHCAL**	**reserved**	**EISPWM**	**EIORLMMC**	**EIORLSIM**	**INTMD**

Field	Bits	Type	Description
EICHV	7	w	Enable interrupt on change of value of bit CHV (charging voltage attached or removed) in register CHST 0 No interrupt enabled 1 Interrupt enabled

CONFIDENTIAL

Field	Bits	Type	Description
EICHMD	6	w	Enable interrupt on change of value of bit CHMD (charging mode change) in register CHST 0 No interrupt enabled 1 Interrupt enabled
EICHCAL	5	w	Enable interrupt on change of value of bit CCAL (current level triggered) in register CHST 0 No interrupt enabled 1 Interrupt enabled
reserved	4	w	Reserved
EISPWM	3	w	Enable interrupt on change of value of bit SPWM (switch-back to PWM mode) in register ISF 0 No interrupt enabled 1 Interrupt enabled
EIORLMMC	2	w	Interrupt on change of value of bit LMMC (regulator LMMC out of regulation) in register ISF 0 No interrupt enabled 1 Interrupt enabled
EIORLSIM	1	w	Interrupt on change of value of bit LSIM (regulator LSIM out of regulation) in register ISF 0 No interrupt enabled 1 Interrupt enabled
INTMD	0	w	Select sensitivenes for edge on INTOUT for signalling an interrupt request to the controller 0 Falling edge 1 Rising edge

INTCTRL2
Interrupt Control Register 2 **(06_H)** **Reset Value: 11011110_B**

7	6	5	4	3	2	1	0
EIOTW	**RAGOTW**	**reserved**	**OTSEN**	**reserved**		**EION**	**DEBUG**

CONFIDENTIAL

Field	Bits	Type	Description
EIOTW	7	w	Enable interrupt on change of value of bit OTW (over-temperature warning interrupt) in register ISF 0 No interrupt enabled 1 Interrupt enabled
RAGOTW	6	w	Reduce audio gain when overtemperature warning occurs 0 Do not reduce audio amplifier gain 1 Reduce audio amplifier gain
reserved	5	w	Reserved
OTSEN	4	w	Overtemperature shutdown sensor enabled 0 Shutdown not enabled 1 Shutdown enabled
reserved	3:2	w	Reserved
EION	1	w	Enables interrupt on change of value of bit LON (level of pin ON) in register ISF 0 No interrupt enabled 1 Interrupt enabled
DEBUG	0	w	0 GEF1 and GEF2 always represent current flag status 1 EF1 and GEF2 store error events. Flags updated after readout

LEDCTRL1
LED Control Register 1 **($0A_H$)** **Reset Value: 00000000_B**

7	6	5	4	3	2	1	0
reserved	**LEDPWM**						**LEDON**

Field	Bits	Type	Description
reserved	7	w	Reserved
LEDPWM	6:1	w	0..63 Duty cycle of LED current = 0.92^{value} for dimming
LEDON	0	w	0 LED driver off 1 LED driver on

CONFIDENTIAL

LEDCTRL2
LED Control Register 2 **(13_H)** **Reset Value: 00001000_B**

7	6	5	4	3	2	1	0
SLED2ON	SLED1ON	LEDCUR			reserved		

Field	Bits	Type	Description
SLED2ON	7	w	0 SLED2 driver off 1 SLED2 driver on
SLED1ON	6	w	0 SLED1 driver off 1 SLED1 driver on
LEDCUR	5:3	w	Set LED driver current = LEDCUR * I_{led0} (see **Table 5-20**) 000 Power down LED driver 001 20 mA 010 40 mA 011 60 mA 100 80 mA 101 100 mA 110 120 mA 111 140 mA
reserved	2:0	w	Reserved

DRVCTRL
Driver Control Register **($0B_H$)** **Reset Value: 00000000_B**

7	6	5	4	3	2	1	0
reserved				VVIB			

Field	Bits	Type	Description
reserved	7:4	w	Reserved
VVIB	3:0	w	**Vibrator driver voltage** Programmable from 0.9 V to 2.0 V in 100 mV steps. See **Table 5-23**. Range: 0000...1100

AUDCTRL2
Audio Control Register 2 **($0C_H$)** **Reset Value: 00000110_B**

7	6	5	4	3	2	1	0
AUDCM			AUDBST		reserved		

Field	Bits	Type	Description
AUDCM	7:5	w	Set audio amplifier common mode voltage (typical value) 000 1.575 V 001 1.650 V 010 1.725 V 011 1.800 V 100 1.875 V 101 1.950 V 110 2.025 V 111 2.100 V
AUDBST	4:3	w	Set audio amplifier amplification to boost mode. Note that boost mode can only be activated when AUDGAIN = 11. 00 Normal operation gain as set by AUDGAIN 01 Normal operation gain as set by AUDGAIN 10 Boost mode, gain = 12 dB 11 Normal operation gain as set by AUDGAIN
reserved	2:0	w	Reserved

AUDCTRL
AUDIO Control Register **($0D_H$)** **Reset Value: 00000010_B**

7	6	5	4	3	2	1	0
reserved			TRISTATE	AUDGAIN		MUTE	AUDON

Field	Bits	Type	Description
reserved	7:5	w	Reserved
TRISTATE	4	w	0 Audio output pulled down to ground in power down 1 Audio output high-ohmic in power down

CONFIDENTIAL

Field	Bits	Type	Description
AUDGAIN	3:2	w	**Set audio gain** 00 Set gain to -6.0 dB automatically used for soft start and in case if bit RAGOTW in register INTCTRL2 is set to 1 and overtemperature warning is triggered 01 Set gain to -1.2 dB 10 Set gain to +2.7 dB 11 Set gain to +7.6 dB
MUTE	1	w	0 Mute off = normal operation 1 Mute on, automatically activated for soft start and all kind of shutdowns
AUDON	0	w	0 Audio amplifier off 1 Audio amplifier on

4.2 Status Registers

All status registers are accessable for read access only.

GEF1
General Error Flag Register 1 (80_H) Reset Value: 00011000_B

7	6	5	4	3	2	1	0
reserved			LRFC	LRF1	LRF2	LANA	LINT

Field	Bits	Type	Description
reserved	7:5	r	Reserved
LRFC	4	r	Current limit exceeded on regulator LRFC
LRF1	3	r	Current limit exceeded on regulator LRF1
LRF2	2	r	Current limit exceeded on regulator LRF2
LANA	1	r	Current limit exceeded on regulator LANA
LINT	0	r	Current limit exceeded on regulator LINT

GEF2
General Error Flag Register 2 (83_H) Reset Value: 00001000_B

7	6	5	4	3	2	1	0
OTWD	reserved			LSIM2	LBB2	LBB1	SDBB

Field	Bits	Type	Description
OTWD	7	r	Overtemperature Warning for Debug Mode
reserved	6:4	r	Reserved
LSIM2	3	r	Current limit exceeded on regulator LSIM2
LBB2	2	r	Current limit exceeded on regulator LBB2
LBB1	1	r	Current limit exceeded on regulator LBB1
SDBB	0	r	Current limit exceeded on DC/DC converter

CONFIDENTIAL

ISF
Interrupt Source Flag Register **(81_H)** **Reset Value: 00000000_B**

7	6	5	4	3	2	1	0
OTW	reserved		LMMC	LSIM	SPWM	OTS	LON

Field	Bits	Type	Description
OTW	7	r	Overtemperature warning
reserved	6:5	r	Reserved
LMMC	4	r	LMMC out of regulation
LSIM	3	r	LSIM out of regulation
SPWM	2	r	Switch-back from PFM to PWM mode triggered by hardware
OTS	1	r	Overtemperature shutdown No interrupt but system reset triggered. After reset it can be checked if OTS was the case.
LON	0	r	Change of level at pin ON

CHST
Charger Status Register **(82_H)** **Reset Value: 00000001_B**

7	6	5	4	3	2	1	0
CHV	CHMD	CCAL	reserved				PMUID

Field	Bits	Type	Description
CHV	7	r	1 $V_{DDCH} > V_{DDCHmin}$ - charging voltage available 0 $V_{DDCH} < V_{DDCHmin}$ - no charging voltage available
CHMD	6	r	1 $V \leq V_{max}$ - current limited charging 0 $V = V_{max}$ - voltage limited charging
CCAL	5	r	1 $I > I_{lim}$ - charging current above limit 0 $I < I_{lim}$ - charging current below limit
reserved	4:1	r	Reserved

CONFIDENTIAL

Field	Bits	Type	Description
PMUID	0	r	Power Management Unit Identification 0 Device is SM-POWER V1.5 1 Device is E-POWERlite

CONFIDENTIAL

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5-1 Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Test Condition
Ambient temperature under bias	T_A	– 40 to 85	°C
Storage temperature	T_{stg}	– 65 to 125	°C
IC supply voltage on pins VDDPW, VDDA, VDDRF	V_{DD}	– 0.3 to 5.5	V
IC supply voltage on pin VDDCH	V_{DDCH}	12.5	V
Voltage on any other pin with respect to ground	V_S	– 0.4 to V_{DD} + 0.4	V
ESD robustness[1)] (HBM: 1.5 kΩ, 100 pF)	$V_{ESD,HBM}$	1000	V

1) According to MIL-Std 883D, method 3015.7 and ESD Ass. Standard EOS/ESD-5.1-1993

Note: Stress above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Operating Range

Table 5-2 Operating Range

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Ambient temperature	T_A	-25	+85	°C	
Supply voltage on pins VDDPW, VDDA, VDDRF, VDDB	V_{BAT}	3.1	4.3	V	Limitations: Devices to operate Ni-MH batteries (V_{BAT}max = 5.2 V) are available on request.
Supply voltage on pin VDDCH	V_{DDCH}	0	12	V	
Ground	V_{SS}	0	0	V	

CONFIDENTIAL

Table 5-2 Operating Range

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Operating Junction Temperature	T_j	-25	120	°C	
Thermal Resistance of Package PG-VQFN-48	R_{thja}	20	t.b.d.	K/W	Depends on PCB layout

Note: In the operating range, the functions given in the circuit description are fulfilled unless otherwise stated.

Note: The electrical characteristics specified in this chapter are ensured over the operating range of the integrated circuit if not restricted in the measurement conditions. Typical characteristics specify mean values exspected over the production spread. Typical characteristics apply at T_A = 25 °C, VBAT = 4 V and VDDCH = 7 V unless otherwise stated.

5.3 Supply Currents

Table 5-3 No Load Supply Currents in Different Modes

Parameter	Symbol	Limit Values			Unit	Test Condition/ Remark
		min.	typ.	max.		
Battery Low Leakage Current	I_{BLL}		2		µA	V_{BAT} < 2.5 V
Shutdown Current	I_{SDO}		20		µA	2.5 V < V_{BAT} < 3.1 V All off except LRTC regulator
Stand-by Mode Current	I_{SB}		200		µA	All pad domains of E-GOLDlite are powered except LSIM2 domain, analog macro and DSP

5.4 AC/DC Characteristics of Common Functions

Table 5-4 Functions concerning the Battery

Parameter	Symbol	Limit Values			Unit	Remark
		min.	typ.	max.		
Undervoltage shutdown (i.e. if battery is plugged out)	V_{BAToff}	2.84	2.90	2.96	V	Voltage measured on pin VDDA
Power-on voltage	V_{BATon}	3.10	3.16	3.22	V	
Capacitance in parallel to battery	C_{BAT}	100		1000	µF	
	f_{Zero}			30	kHz	$f_{Zero} = 1 / (2*pi*C_{BAT}*ESR_{CBAT})$
	ESR	75			mOhm	

Table 5-5 Analog Reference Pins

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Resistor between pin IREF and ground	R_{IREF}	81	82	83	kOhm	
Bypass capacitor at pin BYP	C_{BYP}		68		nF	

Table 5-6 Thermal Management

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Overtemperature shot-down limit	T_{Joff}	125	140	155	°C	
Overtemperature shot-down hysteresis	ΔT_{Joff}		20		°C	
Overtemperature warning	T_{Jwarn}		120		°C	

Table 5-7 Reset Timing

Parameter	Symbol	Limit Values			Unit	Test Condition/ Remark
		min.	typ.	max.		
Internal reset sequence of E-POWERlite (after start of IREF)	t_{resint}	14.4	18	21.6	ms	
INTOUT high while RESETQ low after turn-on of LMMC	t_1	0.8	1	1.2	ms	
INTOUT low while RESETQ low	t_2	26	33	40	ms	
Output RESETQ assertion time after start of LRF2	t_{res}	40.8	51	61.2	ms	$t_{res} = t_{resint} + t_2$

5.5 AC/DC Characteristics of Digital Pins

Table 5-8 AC/DC Characteristics of Digital Signals

Parameter	Symbol	Limit Values		Unit	Test Condition/ Remark
		min.	max.		
Input high level on pin ON to turn on E-POWERlite	V_{IHto}	1.2	V_{BAT} + 0.3	V	
Input high level on pin ON for high level detection with bit LON in register **ISF**	V_{IHdet}	V_{BAT} - 0.9	V_{BAT} - 0.3	V	Battery voltage V_{BAT} = 5.2 V
	V_{IHdet}	V_{BAT} - 0.7	V_{BAT} - 0.3	V	Battery voltage V_{BAT} = 3.2 V
Input low voltage for pin ON	V_{IL}	-0.3	0.3	V	
Output high voltage for pins RESETQ and INTOUT	V_{OH}	V_{RTC} * 0.7	V_{RTC} + 0.3	V	I = 1 mA V_{RTC}: see table **Table**
Input high voltage on pins SDA and SCL[1)]	V_{IH}	V_{INT} * 0.7	V_{INT} + 0.3	V	V_{INT}: see table **Table 5-12**
Input low voltage on pins SDA and SCL[1)]	V_{IL}	-0.3	V_{INT} * 0.3	V	V_{INT}: see table **Table 5-12**

CONFIDENTIAL

Table 5-8 AC/DC Characteristics of Digital Signals

Parameter	Symbol	Limit Values		Unit	Test Condition/ Remark
		min.	max.		
Pulse width of suppressed spikes at SDA and SCL[1)]		0	50	ns	
Hysteresis of Schmitt trigger inputs SDA and SCL[1)]	V_{hys}	V_{INT}*0.1		V	
Output low voltage on pin SDA (open drain)[1)]	V_{OL}	0	0.35	V	I = 3 mA
Output fall time of pin SDA[1)]	t_{of}	20+0.1*CL/ pF	250	ns	Rp[3)] > 5 kOhm
Clock frequency on pin SCL	f_{SCL}	10	406	kHz	
Input high voltage for pin VCXOEN	V_{IH}	V_{DDC}-0.2	V_{BAT}+0.3	V	V_{INT}: see table **Table 5-9**
Input low voltage for pin VCXOEN	V_{IL}	-0.3	0.3	V	

[1)] according to I²C-BUS specification

5.6 AC/DC Characteristics of Power Supply Functions

Table 5-9 Step-Down Converter SDBB

Parameter	Symbol	Limit Values			Unit	Test Condition/ Remark
		min.	typ.	max.		
Internal Oscillator Clock (Switching) Frequency	f_{osc}	400	500	600	kHz	
Resistance of Output Switch	R_{DSON_PMOS}		0.6	0.8	Ohm	
	R_{DSON_NMOS}		0.6	0.8	Ohm	
Inductor		t.b.d	10	t.b.d.	µH	
Output Capacitor		16	22	30	µF	Min. 2 x 10 µF or 1 x 22 µF X5R
Output Capacitor ESR			5	15	mOhm	Min. 2 x 10 µF or 1 x 22 µF X5R

CONFIDENTIAL

Table 5-9 Step-Down Converter SDBB

Parameter	Symbol	Limit Values			Unit	Test Condition/ Remark
		min.	typ.	max.		
Output Voltage under Static load	VDDC1	1.87	1.92	1.97	V	E-GOLD+ V2
	VDDC3	1.75	1.80	1.85	V	S-GOLD, E-GOLD+ V3, E-GOLDlite
	VDDC4	1.46	1.50	1.54	V	
Output Voltage under Dynamic load	VDDC1d	1.80	1.92	2.04	V	See Notes below and **Figure 5-1** to **Figure 5-6**
	VDDC3d	1.68	1.80	1.92	V	
	VDDC4d	1.39	1.50	1.61	V	
Output Current	IVDDC_PWM			400	mA	Normal current limit Load averaged over 10µs !
	IVDDC_PFM			30	mA	
Output Current Change Rate	IVDDC_Up	60			mA / µs	Higher load changes are allowed if restrictions as specified in **Figure 5-1** to **Figure 5-6** are observed
	IVDDC_Down	100			mA / µs	
Ripple Voltage	V_{Rpp_PWM}			12	mV	
	V_{Rpp_PFM}			50	mV	
Efficiency in PWM Mode	Eff_{mload}		92	95	%	50mA < I_{VDDC_PWM} < 300mA maximum Efficiency achieved with $R_{Inductor}$ <= 90mOhm
	Eff_{hload}	85			%	I_{VDDC_PWM} = 600mA
No-Load Current Consumption	IBias_PWM		2.4		mA	
	IBias_PFM		70		µA	

Note: The output voltages under dynamic load as specified in **Table 5-9** *are guaranteed if the maximum output currents, the output current change rates of* **Table 5-9** *and the examples for dynamic behavior on VDDC,* **Figure 5-1** to **Figure 5-6** *are observed.*

Note: The scenario described in **Figure 5-6** *is realistic for emergency shutdowns of the system triggered by overtemperature or undervoltage. If the load drop occurs at*

the absolute worst case of 600 mAthe specified maximum output voltage on VDDC under static load can be exceeded by max. 175 mV (assuming every parameter involved has its worst case). The E-GOLDlite External Bus Unit which is connected to VDDC can take this. The core does not face this overvoltage because it is not directly connected to VDDC. ***Please make sure that the absolute maximum ratings of any external devices attached to VDDC are not violated by this worst case load dump!***

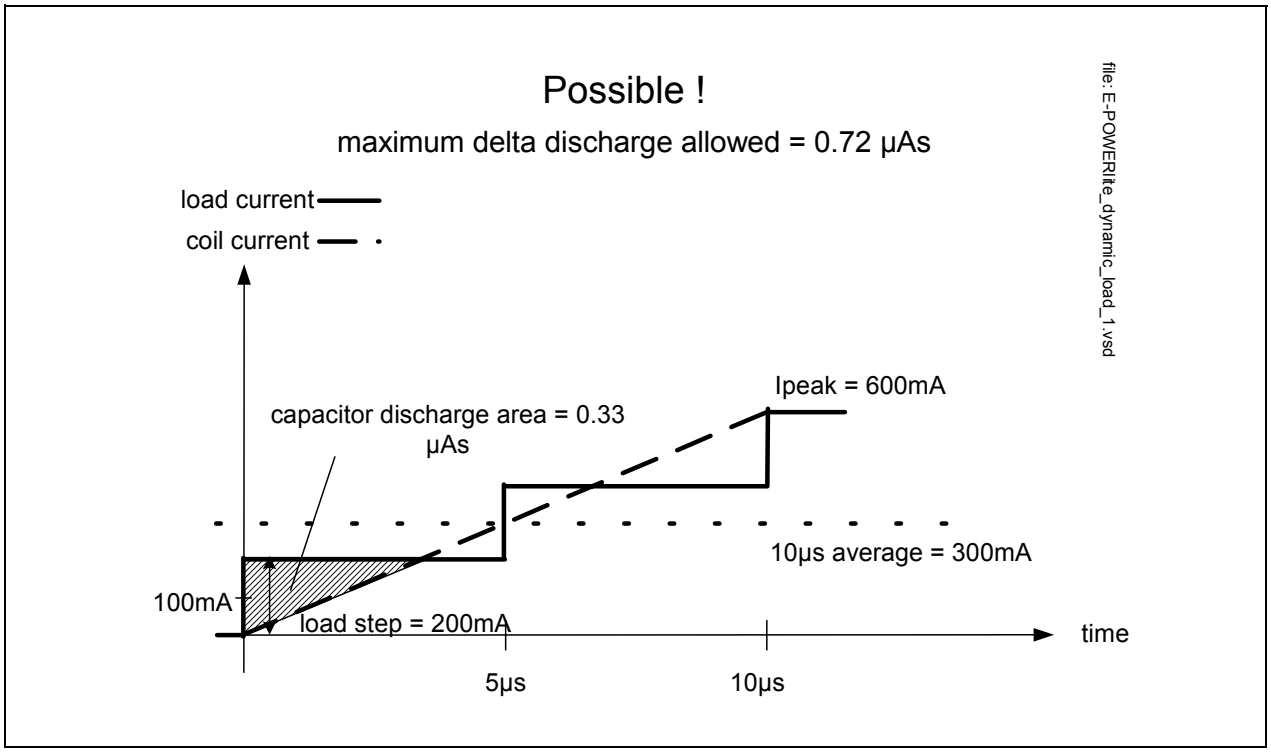

Figure 5-1 Example 1 for Dynamic Load on VDDC

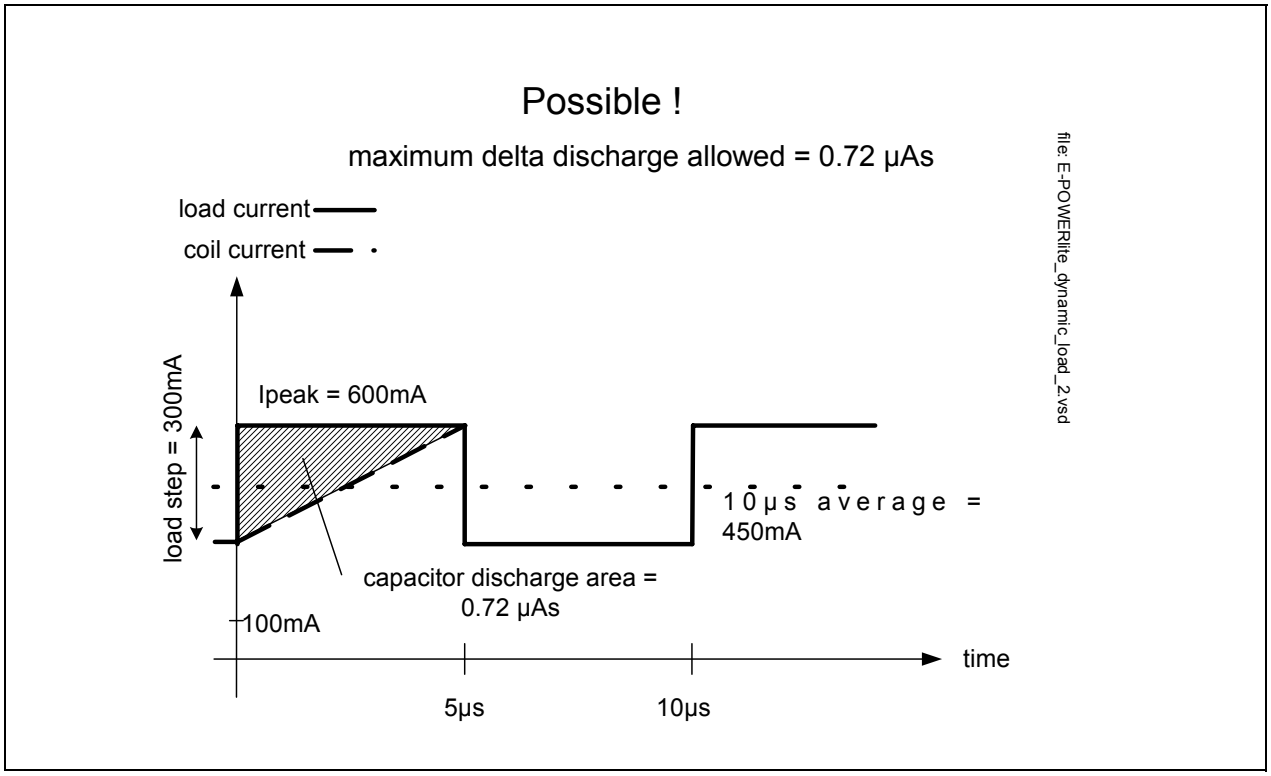

Figure 5-2 Example 2 for Dynamic Load on VDDC

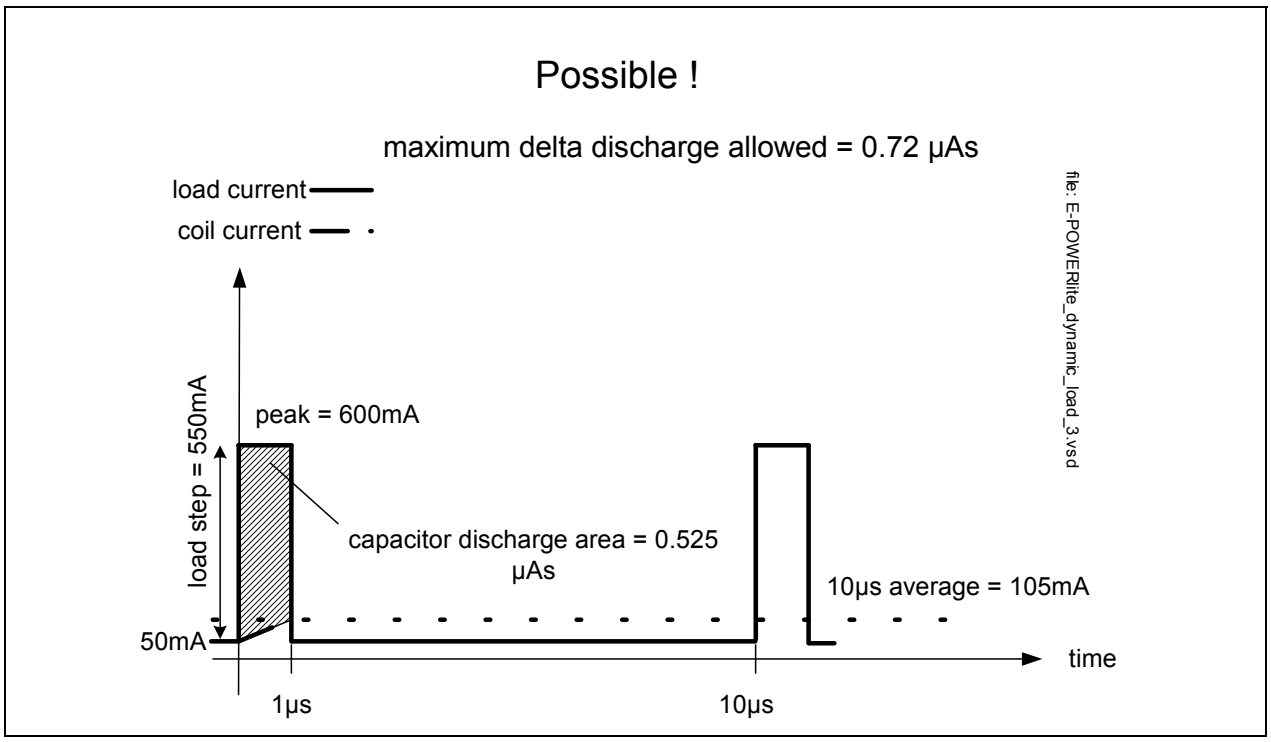

Figure 5-3 Example 3 for Dynamic Load on VDDC

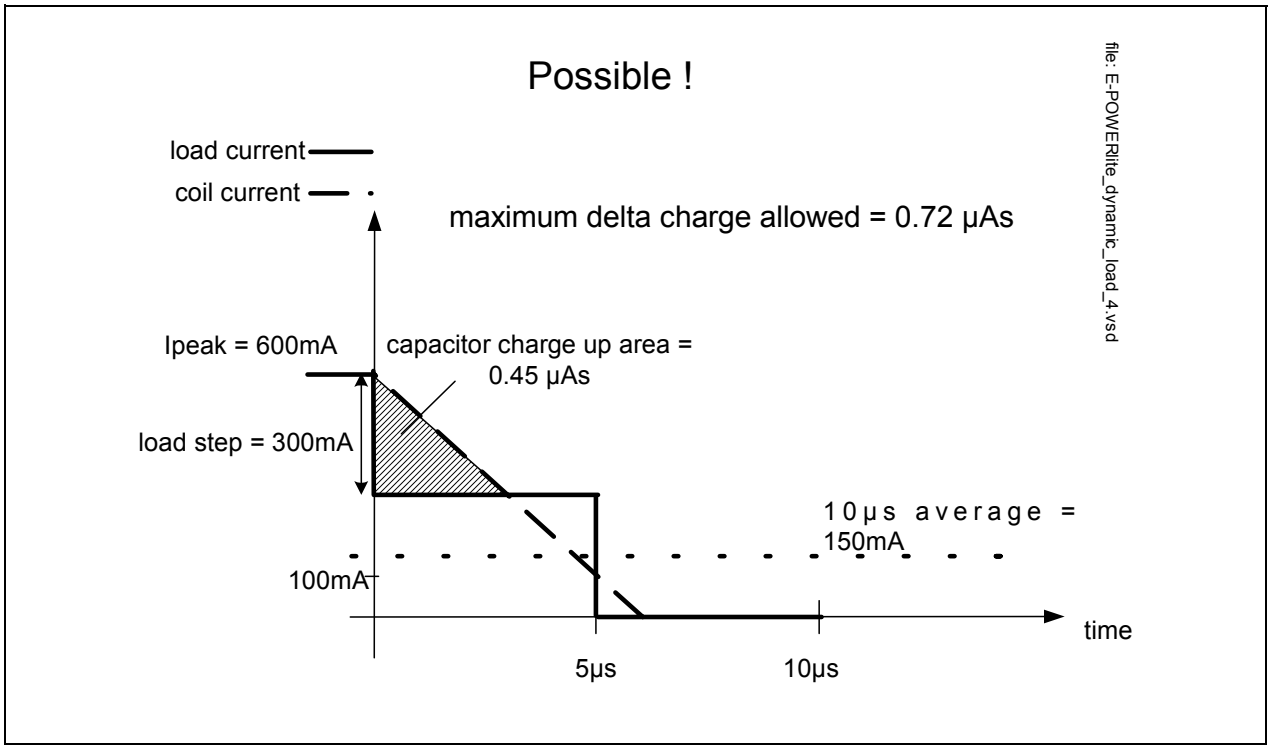

Figure 5-4 Example 4 for Dynamic Load on VDDC

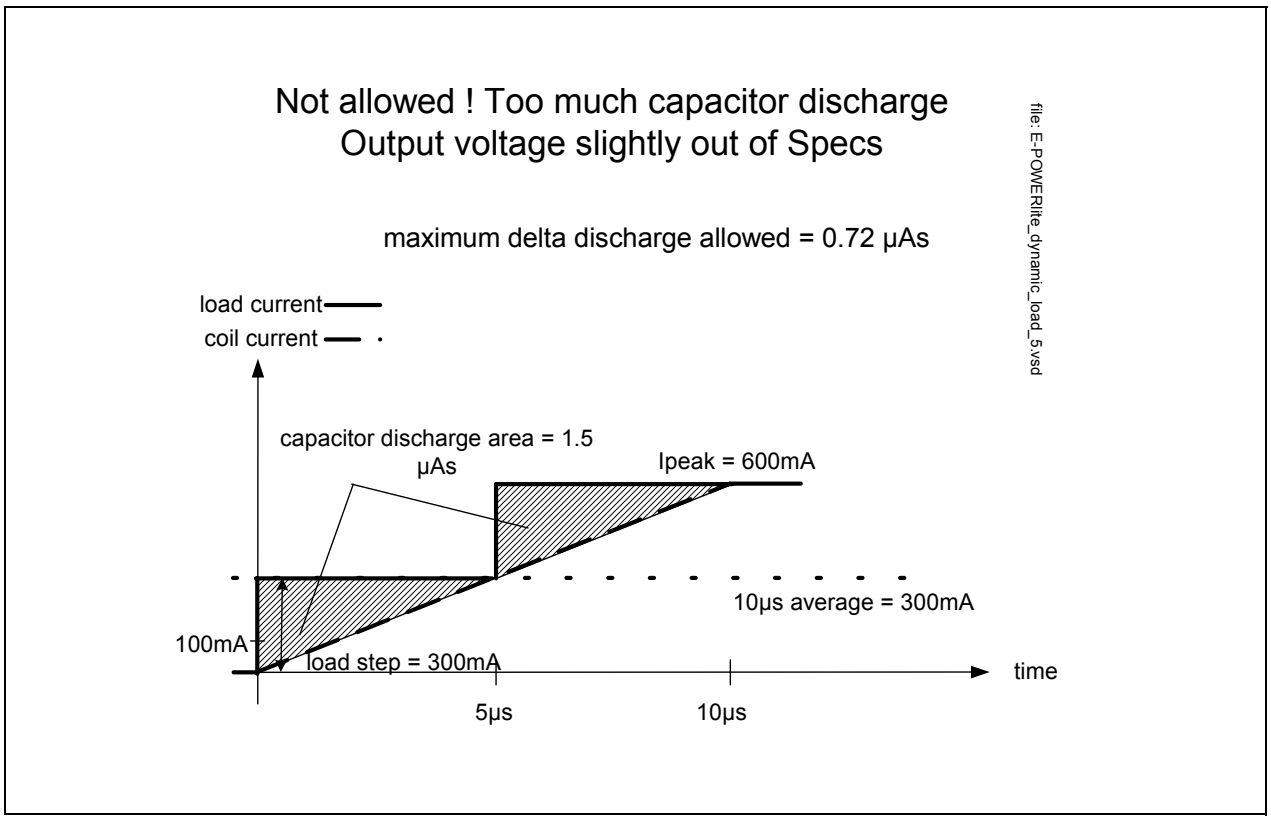

Figure 5-5 Example 5 for Dynamic Load on VDDC

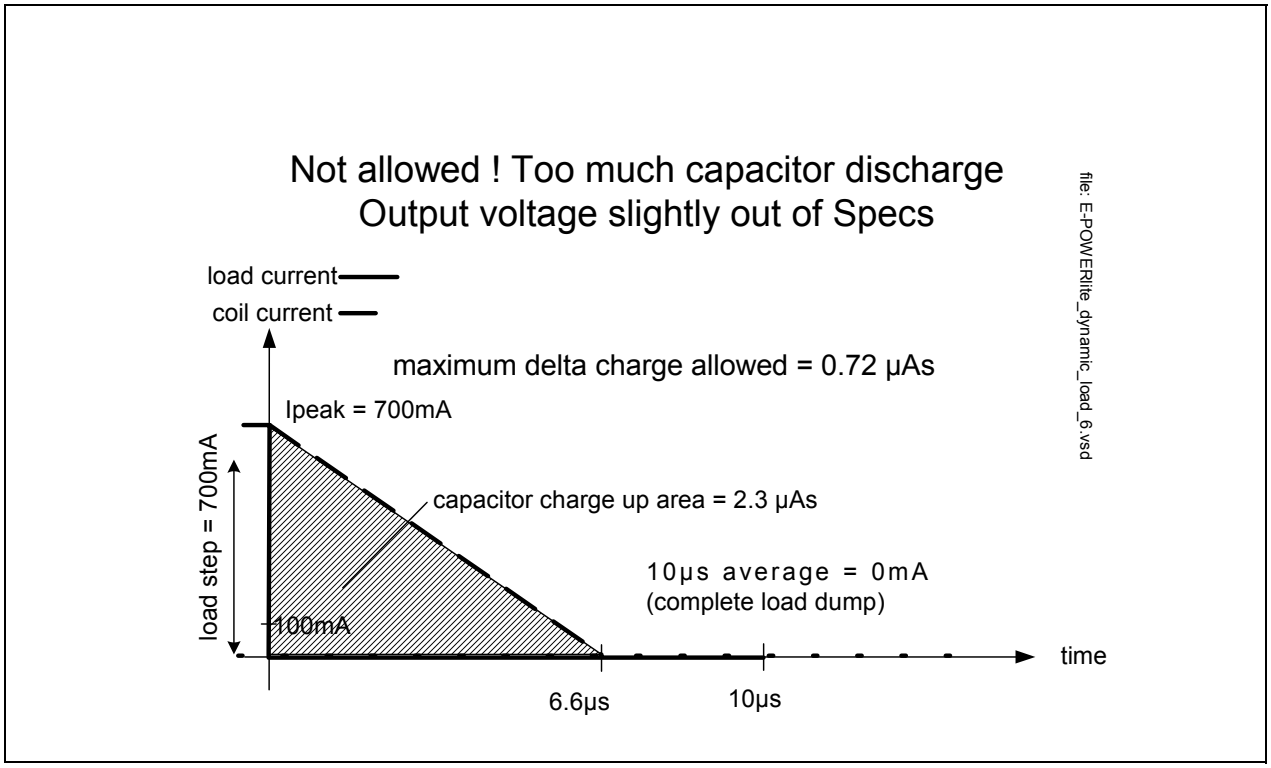

Figure 5-6 Example 6 for Dynamic Load on VDDC

Table 5-10 Linear Regulator LBB1 and LBB2

Parameter	Symbol	Limit Values			Unit	Test Condition/ Remark
		min.	typ.	max.		
Output Voltage under Static Load	V_{LBB1}	1.46	1.5	1.54	V	0 mA < I_{VLBB1}/I_{VLBB2}< $I_{LBB1max}/I_{LBB2max}$
	V_{LBB2}	1.61	1.65[1)]	1.69	V	
Output Voltage under Dynamic Load	V_{LBB1d}	1.41	1.5	1.59	V	Dynamic Load from 1 mA to $I_{LBB1max}/I_{LBB2max}$ C_{out} = 2.2 µF
	V_{LBB2d}	1.56	1.65	1.74	V	
Output current	I_{LBB1} I_{LBB2}			170	mA	
Line Regulation	ΔV_{LNR}		0.15		% / V	C_{out} = 2.2 µF
Load Regulation	ΔV_{LDR}		0.005		% / mA	C_{out} = 2.2 µF
output capacitor	C_{out}	1		2.9	µF	
Series resistance of capacitor on output pin	ESR_C			50	mOhm	

1) This voltage appears if the step down converter is set to 1.92V

Table 5-11 Linear Regulator LANA

Parameter	Symbol	Limit Values			Unit	Test Condition/ Remark
		min.	typ.	max.		
Output Voltage under Dynamic Load	V_{ANAd}	2.56	2.65	2.74	V	Dynamic Load from 1 mA to I_{ANAmax} C_{out} = 2.2 µF
Output Current	I_{ANA}			220	mA	
Power Supply Rejection Ratio C_{out}=2.2 µF, I = 30 mA, ESR_{Cout}= 20 mOhm	$PSRR_1$	48	54		dB	100 Hz
	$PSRR_2$	48	54			1 kHz
	$PSRR_3$	36	42			10 kHz
	$PSRR_4$	28	33.5			100 kHz
Line Regulation	ΔV_{LNR}		0.15		% / V	C_{out} = 2.2 µF
Load Regulation	ΔV_{LDR}		0.005		% / mA	C_{out} = 2.2 µF
output capacitor	C_{out}	1.5		5.5	µF	
series resistance of capacitor on output pin	ESR_C			50	mOhm	
Quiescent current	I_{qc}		110		µA	
Shutdown reverse current (flowing into pin VANA)	I_{SDrev}		10		µA	LANA turned off

Table 5-12 Linear Regulator LINT

Parameter	Symbol	Limit Values			Unit	Test Condition/ Remark
		min.	typ.	max.		
Output Voltage under Dynamic Load	V_{INTd}	2.62	2.72	2.82	V	Dynamic Load from 1 mA to $I_{INT-max}$ C_{out} = 2.2 µF
Output Current	I_{INT}			135	mA	

CONFIDENTIAL

Table 5-12 Linear Regulator LINT

Parameter	Symbol	Limit Values			Unit	Test Condition/ Remark
		min.	typ.	max.		
Allowed load change rate in standby mode to keep voltage in SPECs	$Ldcr_{st-dby}$	no restriction				Dynamic Load from 0 to 10 mA
				3	mA/µs	Dynamic Load above 10 mA to I_{INTmax} / Assuming C_{out} = min
output capacitor	C_{out}	1		4.3	µF	
series resistance of capacitor on output pin	ESR_C			50	mOhm	

Table 5-13 Linear Regulator LSIM and LMMC

Parameter	Symbol	Limit Values			Unit	Test Condition/ Remark
		min.	typ.	max.		
Output Voltage under Dynamic Load	V_{SIM1d} V_{MMCd}	2.75	2.85	2.95	V	Dynamic Load from 1 mA to I_{SIMmax}/I_{MMCmax} C_{out} = 1.5 µF
		1.71	1.8	1.95		
Output current	I_{SIM1} I_{MMC}			22	mA	
Line Regulation	ΔV_{LNR}		0.15		% / V	C_{out} = 1.5 µF
Load Regulation	ΔV_{LDR}		0.005		% / mA	C_{out} = 1.5 µF
Allowed load change rate in standby mode to keep voltage in SPECs	$Ldcr_{stdby}$	no restriction				Dynamic Load from 0 to 7 mA
				2	mA/µs	Dynamic Load above 7 mA to I_{SIMmax} /I_{MMCmax} assuming C_{out} = min
Output capacitor	C_{out}	0.68		2.9	µF	
Series resistance of capacitor on output pin	ESR_C			50	mOhm	

Table 5-14 Linear Regulator LSIM2

Parameter	Symbol	Limit Values			Unit	Test Condition/ Remark
		min.	typ.	max.		
Output Voltage under Dynamic Load	V_{SIM1d}	2.75	2.85	2.95	V	Dynamic Load from 1 mA to I_{SIMmax} C_{out} = 2.2 µF
		1.71	1.8	1.95		
Output current	I_{SIM2}			200	mA	
Line Regulation	ΔV_{LNR}		0.15		% / V	C_{out} = 2.2 µF
Load Regulation	ΔV_{LDR}		0.005		% / mA	C_{out} = 2.2 µF
Allowed load change rate in standby mode to keep voltage in SPECs	$Ldcr_{stdby}$	no restriction				Dynamic Load from 0 to 15 mA
				4.5	mA/µs	Dynamic Load above 15 mA to $I_{SIM2max}$ / Assuming C_{out} = min
Output capacitor	C_{out}	1.5		4.3	µF	
Series resistance of capacitor on output pin	ESR_C			50	mOhm	

Table 5-15 Linear Regulator LRFC

Parameter	Symbol	Limit Values			Unit	Test Condition/ Remark
		min.	typ.	max.		
Output Voltage under Dynamic Load	V_{RFCd}	1.40	1.50	1.60	V	Dynamic Load from 1 mA to I_{RF0max} C_{out} = 2.2 µF
Output Current	I_{RFC}			120	mA	
Output Noise Voltage	V_{Noise}		40		μV_{RMS}	BW = 10 Hz to 100 kHz @ half nominal load C_{out} = 2.2 µF

CONFIDENTIAL

Table 5-15 Linear Regulator LRFC

Parameter	Symbol	Limit Values			Unit	Test Condition/ Remark
		min.	typ.	max.		
Power Supply Rejection Ratio (for 1.5 Volt mode only) C_{out}=2.2 µF, I = 30 mA, ESR_{Cout}= 20 mOhm	$PSRR_1$	50	54		dB	100 Hz
	$PSRR_2$	50	54			1 kHz
	$PSRR_3$	37	42			10 kHz
	$PSRR_4$	30	33.5			100 kHz
Line Regulation	ΔV_{LNR}		0.15		% / V	C_{out} = 2.2 µF
Load Regulation	ΔV_{LDR}		0.005		% / mA	C_{out} = 2.2 µF
Output capacitor	C_{out}	1		4.3	µF	
Series resistance of capacitor on output pin	ESR_C			50	mOhm	
Quiescent current	I_{qc}		50		µA	

Table 5-16 Linear Regulator LRF1

Parameter	Symbol	Limit Values			Unit	Test Condition/ Remark
		min.	typ.	max.		
Output Voltage under Dynamic Load	V_{RF1d}	2.40	2.50	2.60	V	Dynamic Load from 1 mA to I_{RF1max} C_{out} = 2.2 µF
Output Current	I_{RF1max}			120	mA	
Output Voltage Noise Density	V_{Noise}		40		μV_{RMS}	BW = 10 Hz to 100 kHz @ half nominal load C_{out} = 2.2 µF
Power Supply Rejection Ratio C_{out}=2.2 µF, I = 30 mA, ESR_{Cout}= 20 mOhm	$PSRR_1$	48	54		dB	100 Hz
	$PSRR_2$	48	54			1 kHz
	$PSRR_3$	36	42			10 kHz
	$PSRR_4$	28	33.5			100 kHz
Line Regulation	ΔV_{LNR}		0.15		%/V	C_{out} = 2.2 µF
Load Regulation	ΔV_{LDR}		0.005		%/mA	C_{out} = 2.2 µF
Output capacitor	C_{out}	1.5		5.5	µF	
Series resistance of capacitor on output pin	ESR_C			50	mOhm	

CONFIDENTIAL

Table 5-16 Linear Regulator LRF1

Parameter	Symbol	Limit Values			Unit	Test Condition/ Remark
		min.	typ.	max.		
Quiescent current	I_{qc}		110		µA	
Shutdown reverse current (flowing into pin VRF1)	I_{SDrev}		10		µA	LRF1 turned off

Table 5-17 Linear Regulator LRF2

Parameter	Symbol	Limit Values			Unit	Test Condition/ Remark
		min.	typ.	max.		
Output Voltage under Dynamic Load	V_{RF2d}	2.60	2.70	2.80	V	Dynamic Load from 1 mA to I_{RF2max} C_{out} = 2.2 µF
		2.40	2.50	2.60		
Output Current	I_{RF2}			15	mA	
Output Voltage Noise Density	V_{Noise}		40		μV_{RMS}	BW = 10 Hz to 100 kHz @ half nominal load C_{out} = 2.2 µF
Power Supply Rejection Ratio C_{out}=2.2 µF, I = 3 mA, ESR_{Cout}= 20 mOhm	$PSRR_1$	50	54		dB	100 Hz
	$PSRR_2$	50	54			1 kHz
	$PSRR_3$	37	42			10 kHz
	$PSRR_4$	30	33.5			100 kHz
Line Regulation	ΔV_{LNR}		0.15		%/V	C_{out} = 2.2 µF
Load Regulation	ΔV_{LDR}		0.005		%/mA	C_{out} = 2.2 µF
output capacitor	C_{out}	0.68		4.3	µF	
Series resistance of capacitor on output pin	ESR_C			50	mOhm	
Shutdown reverse current (flowing into pin VRF2)	I_{SDrev}		10		µA	LRF2 turned off

Table 5-18 Linear Regulator LRTC

Parameter	Symbol	Limit Values			Unit	Test Condition/ Remark	
		min.	typ.	max.		V_{BATmin}	I_{RTC}
Output Voltage	V_{RTC}	2.01	2.11	2.21	V	3.0 V	0 µA
		1.95	2.05	2.15	V		300 µA
Drop-out Voltage V_{BAT} - V_{RTC}	$V_{BATRTCon}$			0.9	V		0 µA
Output current	I_{RTC}	300			µA	V_{BAT} > 3.0 V	
Reverse Current	I_{rev}		1		µA	V_{BAT} = 0V	
Capacitance on pin VRTC	C_{VRTC}	10		220	µF		
Turn-On Voltage	$V_{BATRTCon}$	2.20	2.50	2.80	V		

5.7 AC/DC Characteristics of Audio Amplifier

Table 5-19 Audio Amplifier

Parameter	Symbol	Limit Values			Unit	Test Condition/ Remark
		min.	typ.	max.		
Signal frequencies	f_{sig}	20	1k	20k	Hz	
Output voltage full scale differential peak-to-peak	$V_{outdpp}FS$		5.06		V	Sine wave
Input voltage full scale differential peak-to-peak	$V_{indpp}FS$			5.50	V	Square wave gain set = -1.2dB
Input voltage full scale differential peak-to-peak	$V_{indpp}FS$			3.70	V	Sine wave gain set = 2.7dB Higher than max. value may cause distortion
Input voltage full scale differential peak-to-peak	$V_{indpp}FS$			2.10	V	Sine wave gain set = 7.6dB Higher than max. value may cause distortion

CONFIDENTIAL

Table 5-19 Audio Amplifier

Parameter	Symbol	Limit Values			Unit	Test Condition/ Remark
		min.	typ.	max.		
Input voltage full scale differential peak-to-peak	$V_{indpp}FS$			1.27	V	Sine wave gain set = 12dB Higher than max. value may cause distortion
Selectable output common mode voltages	V_{outcm}					recommended for V_{BAT} range:
			1.575		V	< 3.225 V
			1.65		V	3.225 V - 3.375 V
			1.725		V	3.375 V - 3.525 V
			1.8		V	3.525 V - 3.675 V
			1.875		V	3.675 V - 3.825 V
			1.95		V	3.825 V - 3.975 V
			2.025		V	3.975 V - 4.125 V
			2.1		V	> 4.125 V
Output power (voice)	P_{out}voice		400		mW	V_{BAT} = 3.3 V R_L = 8 Ohm V_{in}diffpp = 3.7 V sine wave 1 kHz gain set = 2.7 dB
Output power (digital ringing)	P_{out}dring		660		mW	V_{BAT} = 3.3 V R_L = 8 Ohm V_{in}diffpp = 5.3 V +/- 3.5 % square wave gain set = -1.2 dB

CONFIDENTIAL

Table 5-19 Audio Amplifier

Parameter	Symbol	Limit Values			Unit	Test Condition/ Remark
		min.	typ.	max.		
Max. output power(ringing)	P_{out}ring		500		mW	V_{BAT} = 3.3 V R_L = 8 Ohm V_{in}diffpp =2.4 V sine wave 1kHz gain set = 7.6 dB **AUDCM** = 001
			600		mW	V_{BAT} = 3.6 V R_L = 8 Ohm V_{in}diffpp =2.6 V sine wave 1kHz gain set = 7.6 dB **AUDCM** = 011
			720		mW	V_{BAT} = 3.9 V R_L = 8 Ohm V_{in}diffpp =2.8 V sine wave 1kHz gain set = 7.6 dB **AUDCM** = 101
			850		mW	V_{BAT} = 4.2 V R_L = 8 Ohm V_{in}diffpp =3.1 V sine wave 1kHz gain set = 7.6 dB **AUDCM** = 111
Maximum output current	I_{max}			570	mA	R_L = 7 Ohm

CONFIDENTIAL

Table 5-19 Audio Amplifier

Parameter	Symbol	Limit Values			Unit	Test Condition/ Remark
		min.	typ.	max.		
Power supply rejection ratio	PSRR	54	60		dB	150 mV_{p-p} @ 217 Hz Sinewave V_{BAT} = 3.3 V gain set = 2.7 dB Input shorted at common mode voltage
		56	62		dB	150 mV_{p-p} @ 1 kHz Sinewave V_{BAT} = 3.3 V gain set = 2.7 dB Input shorted at common mode voltage
Distortion Factor	DF		0.3		%	V_{BAT} = 3.3 V gain set = 2.7 dB P_{out}voice = 400mW R_L = 8 Ohm f_{sig} = 1 kHz 20 Hz to 20 kHz
Total Harmonic Distortion	THD		66		dB	V_{BAT} = 4 V gain set = 2.7 dB P_{out}voice = 400mW R_L = 8 Ohm f_{sig} = 1 kHz 20 Hz to 20 kHz
Absolute Gain Error		-6.2	-6.0	-5.8	dB	f_{sig} = 1 kHz
		-1.4	-1.2	-1.0		
		2.5	2.7	2.9		
		7.4	7.6	7.8		
Relative Gain Error 20kHz to 1kHz			-0.1		dB	f_{sig} = 1 kHz, 20kHz
Input impedance		8			kOhm	
Quiescent current	I_Q		4	10	mA	
Output differential ohmic load	R_L	7		16	Ohm	

CONFIDENTIAL

Table 5-19 Audio Amplifier

Parameter	Symbol	Limit Values			Unit	Test Condition/ Remark
		min.	typ.	max.		
Output differential capacitive load	C_L			2000	pF	
Duration of internal shut-down sequence (to avoid click & pop)	t_{sd}			154	µs	

5.8 AC/DC Characteristics of Driver Functions

Table 5-20 LED Driver

Parameter	Symbol	Limit Values			Unit	Test Cond. / Remark
		min.	typ.	max.		
Output current on pin LED	I_0			1	µA	LEDCUR = 0 or LEDON = 0
	I_{led0}	18.6	20.0	22.5	mA	320 mV < V_{LED} < V_{BAT} - 1.4 V T_j = 0 ... 100° C R_{IREF} = 82k
	I_{led}	LEDCUR * I_{led0}			mA	LEDCUR = 1...7
Voltage on pin LED				5.2	V	

Table 5-21 SLED1 Driver

Parameter	Symbol	Limit Values			Unit	Test Cond. / Remark
		min.	typ.	max.		
Output current on pin SLED1	I_0			1	µA	SLED1ON = 0
	I_{out}	6.4	7.5	8.6	mA	V_{SLED1} > 400 mV
		5.25	7.5	9.75	mA	only during precharge phase V_{BAT} > 2.2 V V_{SLED1} > 400 mV
Voltage on pin SLED1				5.2	V	

CONFIDENTIAL

Table 5-22 SLED2 Driver

Parameter	Symbol	Limit Values			Unit	Test Cond. / Remark
		min.	typ.	max.		
Output current on pin SLED2	I_0			1	µA	SLED2ON = 0
	I_{out}	6.4	7.5	8.6	mA	V_{SLED2} > 400 mV
Voltage on pin SLED2				5.2	V	

Table 5-23 Vibrator Motor Driver

Parameter	Symbol	Limit Values			Unit	Test Cond. / Remark
		min.	typ.	max.		
Output voltage on pin VIB	V_0		0		V	VVIB = 0h
	V_{out}	0.85	0.9	0.95		VVIB = 1h
		0.95	1.0	1.05		VVIB = 2h
		1.05	1.1	1.15		VVIB = 3h
		1.14	1.2	1.26		VVIB = 4h
		1.24	1.3	1.36		VVIB = 5h
		1.33	1.4	1.47		VVIB = 6h
		1.43	1.5	1.57		VVIB = 7h
		1.52	1.6	1.68		VVIB = 8h
		1.62	1.7	1.78		VVIB = 9h
		1.71	1.8	1.89		VVIB = Ah
		1.81	1.9	1.99		VVIB = Bh
		1.90	2.0	2.10		VVIB = Ch
Output current on pin VIB	I_{out}			100[1)]	mA	
Bypass capacitor on pin VIB	C_{out}	0		10	nF	

[1)] in case of a short circuit the current will be limited to about 220mA typical

CONFIDENTIAL

Table 5-24 Charge Control Functions

Parameter	Symbol	Limit Values			Unit	Test Cond. / Remark
		min.	typ.	max.		
Maximum charging voltages T_A = 0° ... 50° C T_J = 0° ... 90° C	V_{CHmax1}	4.06	4.10	4.14	V	Li-Ion batteries Overcharge Safety Function in battery block recommended
	V_{CHmax2}	4.17	4.20	4.23	V	Li-Ion batteries Overcharge Safety Function in battery block recommended
	V_{CHmax3}	5.10	5.15	5.20	V	Ni-MH batteries (See 5.2 “Operating Range” on page 61.)
Valid voltage of AC-adapter	VDDCHmin	3.52	3.6	3.71	V	Upper limit of hysteresis
Not valid voltage of AC-adapter		3.32	3.4	3.51	V	
Hysteresis between on-off		0.17		0.22	V	
Charging current from AC-adapter	$I_{ACAdapt}$	400		1200	mA	$I_{ACAdaptmax}$ = maximum current from AC-adapter
Internal charging current limiting levels	I_{CHClim}	364	400	436	mA	CHCLIM = 0h
		455	500	545		CHCLIM = 1h
		546	600	654		CHCLIM = 2h
		637	700	763		CHCLIM = 3h
		728	800	872		CHCLIM = 4h
		819	900	981		CHCLIM = 5h
		910	1000	1090		CHCLIM = 6h
		1000	1100	1200		CHCLIM = 7h
Transconductance of external PMOS Transistor	gm	0.311		5.850	A / V	I_{drain}PMOS = 18 mA (idle mode) ... full current of AC-adapter

CONFIDENTIAL

Parameter	Symbol	Limit Values			Unit	Test Cond. / Remark
		min.	typ.	max.		
Tolerance of voltage measurements across the current sense resistor	$\Delta V_R/V_R$			10	%	Test condition: R=0.15 Ohm ± 1% Remark: whichever value is bigger
	ΔV_R			4	mV	
Current sense resistor	R_{sense}		0.15		Ohm	1% tolerance
Pre-charge turn-on voltage (low hysteretical limit)	V_{PREmin}	3.10	3.25	3.40	V	
Pre-charge turn-off voltage(high hysteretical limit)	V_{PREmax}	3.35	3.50	3.65	V	
Min. hysteresis between V_{PREmin} and V_{PREmax}	ΔV_{PR}	200			mV	
Precharging current	I_{Prech1} I_{Prech2}	40 96	60 120	80 144	mA	Li-Ion batteries overcharge safety function in battery block recommended

Note: If VDDCHmin is not reached neither precharging nor normal charging is possible. This is pevented by an internal protection circuit.

a) If VDDCHmin is reached and an interrupt is generated for the controller it is highly recommended to do two consecutive readings of the CHST register. The first read operation will clear all interrupt events for the flags CHV, CHMD and CCAL. The second read operation will show the present status of the register.

6 Package Information

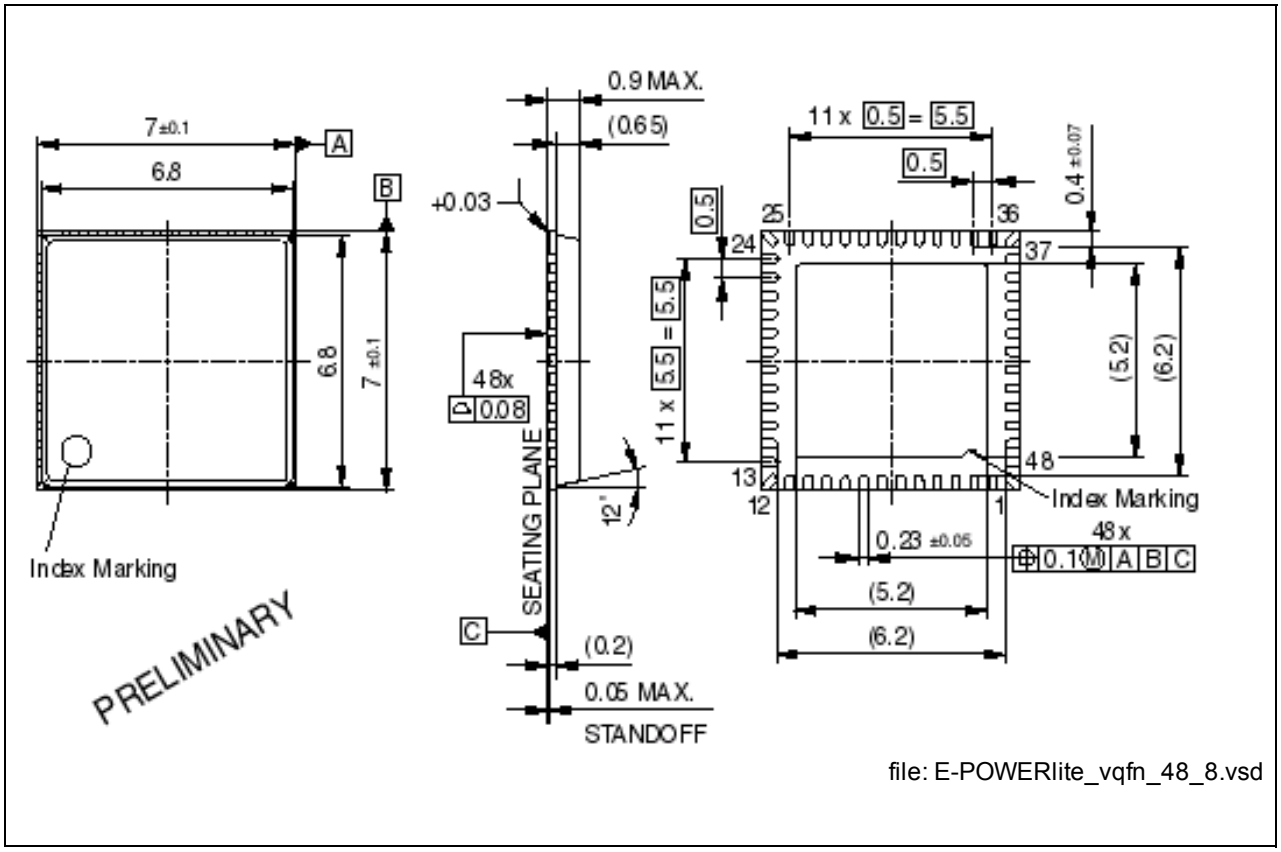

Figure 6-1 PG-VQFN-48-4

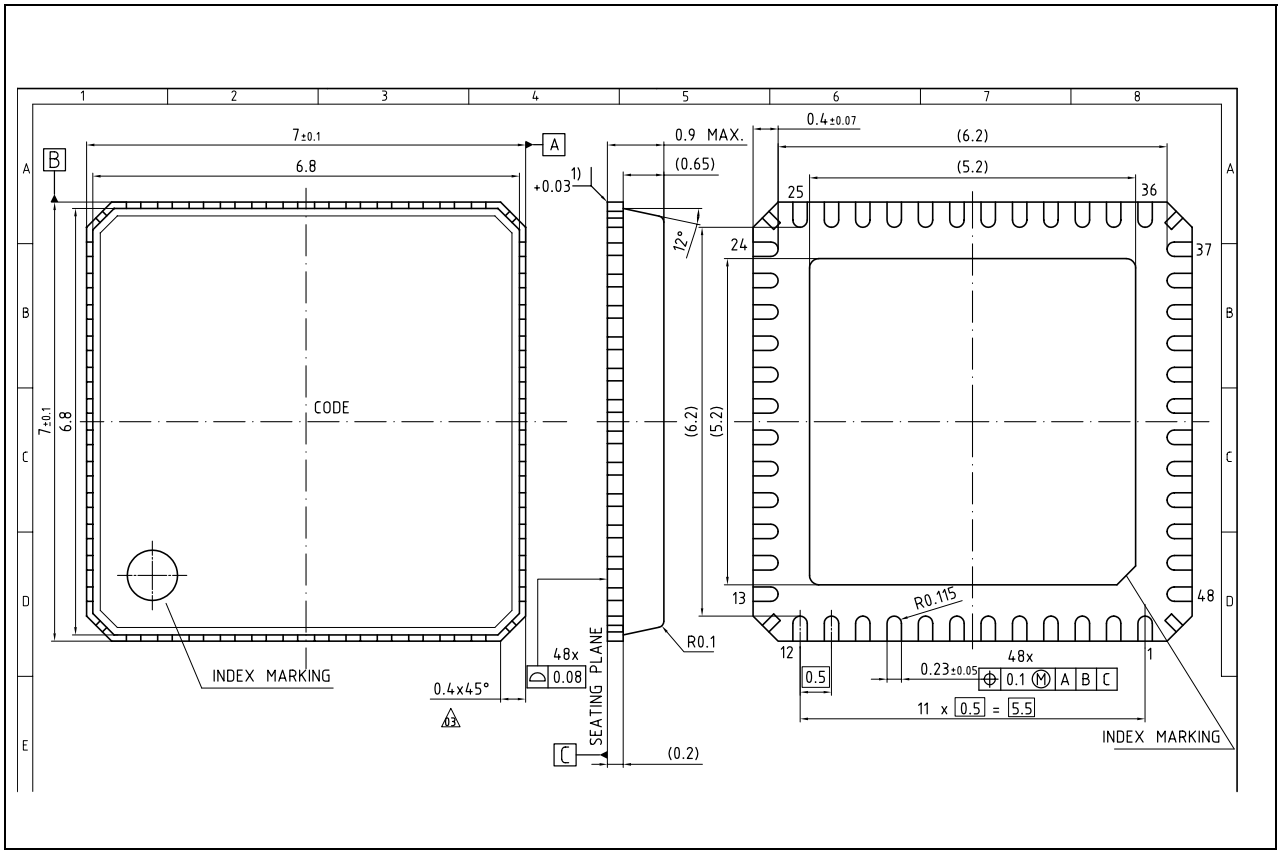

Figure 6-2 PG-VQFN-48-15

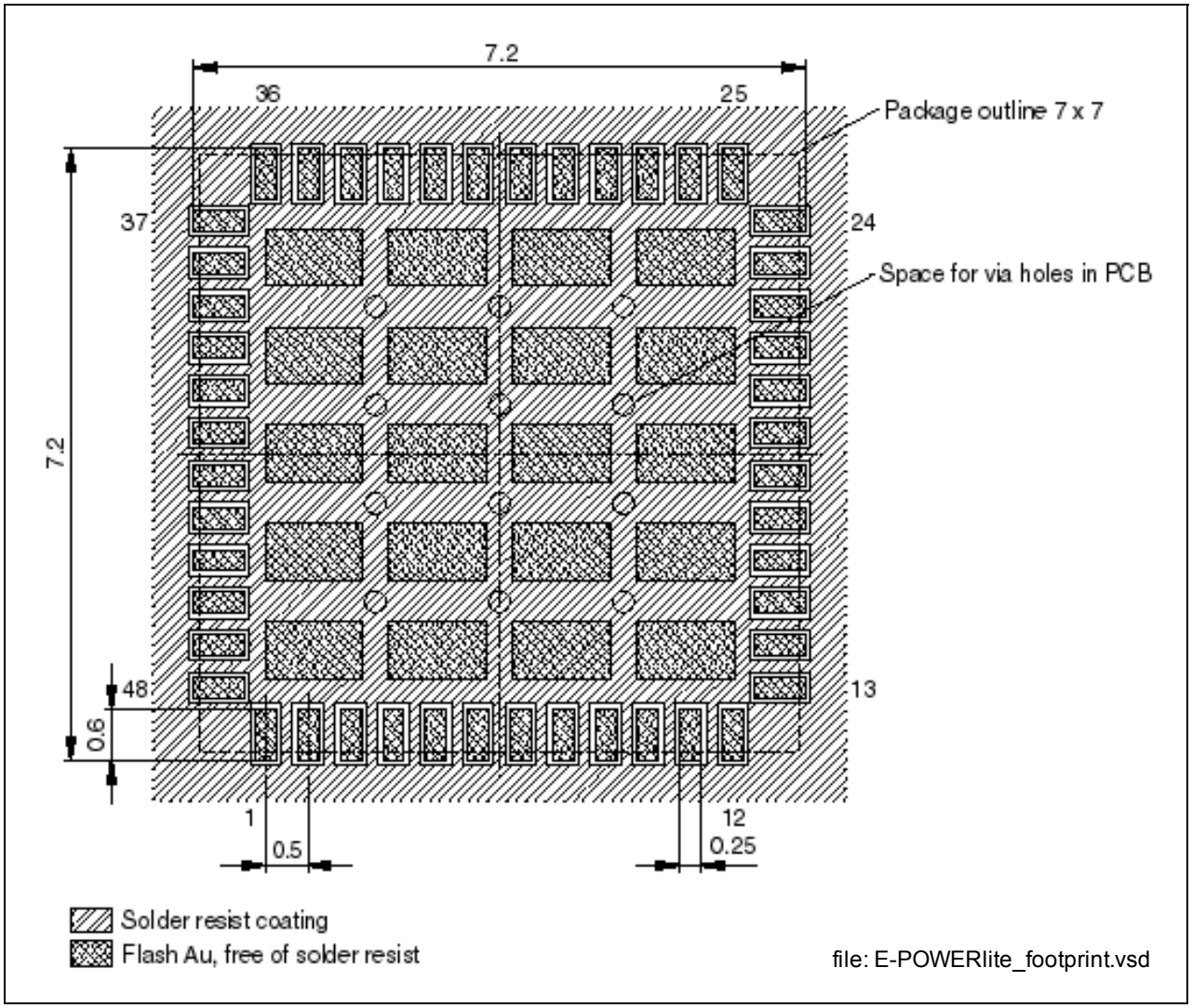

Figure 6-3 PG-VQFN-48-4/PG-VQFN-48-15 Footprint

Total Quality Management

Qualität hat für uns eine umfassende Bedeutung. Wir wollen allen Ihren Ansprüchen in der bestmöglichen Weise gerecht werden. Es geht uns also nicht nur um die Produktqualität – unsere Anstrengungen gelten gleichermaßen der Lieferqualität und Logistik, dem Service und Support sowie allen sonstigen Beratungs- und Betreuungsleistungen.

Dazu gehört eine bestimmte Geisteshaltung unserer Mitarbeiter. Total Quality im Denken und Handeln gegenüber Kollegen, Lieferanten und Ihnen, unserem Kunden. Unsere Leitlinie ist jede Aufgabe mit „Null Fehlern“ zu lösen – in offener Sichtweise auch über den eigenen Arbeitsplatz hinaus – und uns ständig zu verbessern.

Unternehmensweit orientieren wir uns dabei auch an „top“ (Time Optimized Processes), um Ihnen durch größere Schnelligkeit den entscheidenden Wettbewerbsvorsprung zu verschaffen.

Geben Sie uns die Chance, hohe Leistung durch umfassende Qualität zu beweisen.

Wir werden Sie überzeugen.

Quality takes on an allencompassing significance at Semiconductor Group. For us it means living up to each and every one of your demands in the best possible way. So we are not only concerned with product quality. We direct our efforts equally at quality of supply and logistics, service and support, as well as all the other ways in which we advise and attend to you.

Part of this is the very special attitude of our staff. Total Quality in thought and deed, towards co-workers, suppliers and you, our customer. Our guideline is “do everything with zero defects”, in an open manner that is demonstrated beyond your immediate workplace, and to constantly improve.

Throughout the corporation we also think in terms of Time Optimized Processes (top), greater speed on our part to give you that decisive competitive edge.

http://www.infineon.com

Published by Infineon Technologies AG