# Globe6 RF System

Massimo Vlacci 18 February 2006

### **Globe6 RF System**

- 1. RF System Overview
- 2. Receiver
- 3. Front-End Module
- 4. Transmitter
- 5. Digitally Controlled XO
- 6. Register setting

#### **GSM/GPRS** Basic Platform

Infineon chipset key componets:

■ E-GOLDradio PMB7870

GSM/GPRS **Single Chip** Solution integrates Baseband System and GSM850/E-GSM/DCS/PCS Quad-Band RF Transceiver for voice and data applications

■ PASi-G PMB6293

Quad-Band GSM850/E-GSM/DCS/PCS **Power Amplifier** Module based on 0.13µm

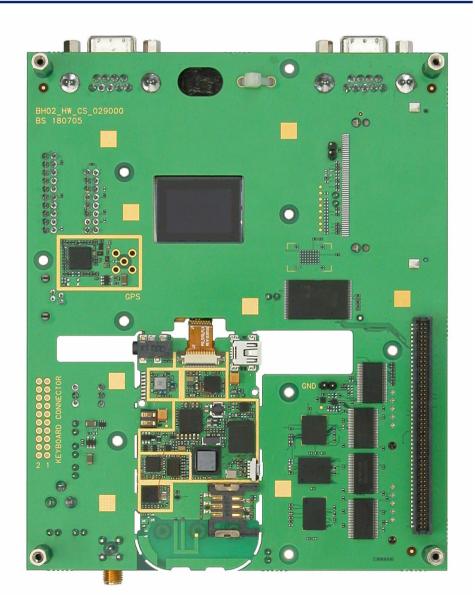
CMOS technology, with integrated power controller

■ E-POWERlite PMB6814

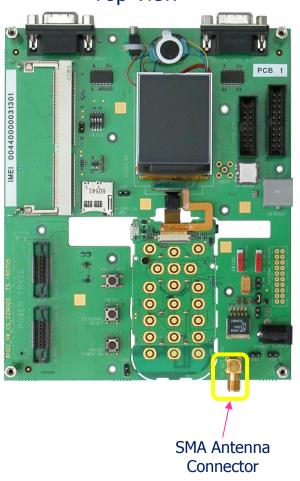
Power Management Unit

■ BlueMoon UniCellular PMB8753

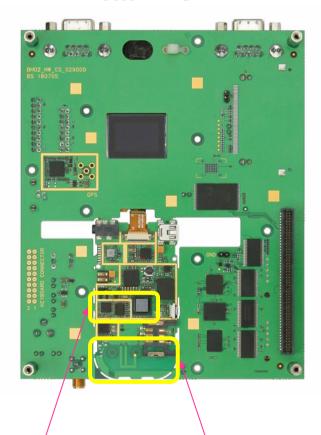
Single-Chip Bluetooth 2.0 + EDR



#### Top View



#### **Bottom View**



**Printed** 

Antenna

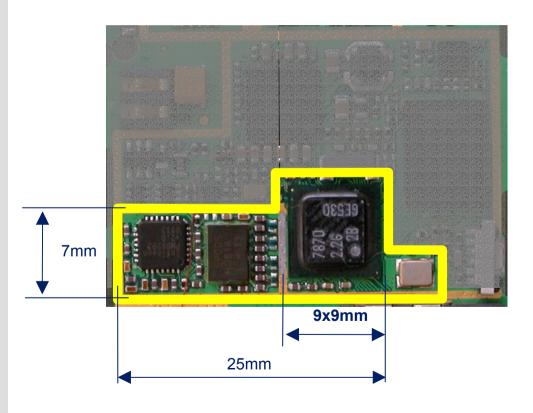
**GSM** 

Transceiver

#### Quad-Band Transceiver on Globe6:

# Location on board

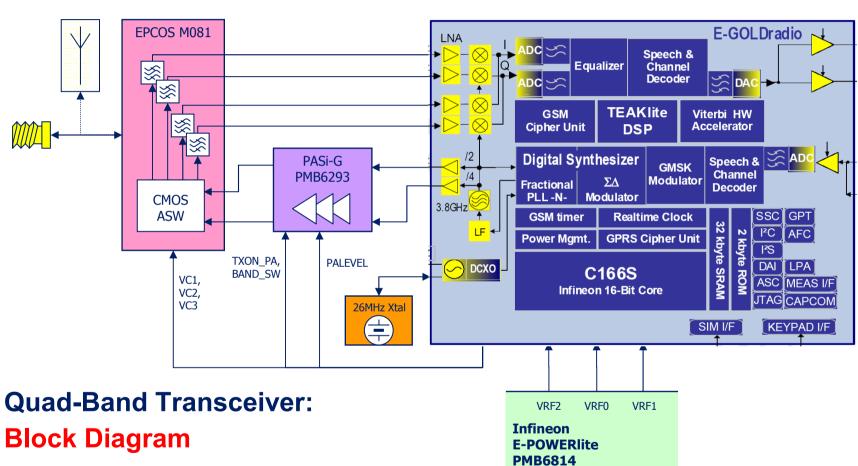
# The Globe6 implements the leading-edge solution for 2G GSM/GPRS RF Transceiver



- Quad-Band
- GPRS class 12
- 40 components total (including 12 passives for RX matching)
- 6-layers PCB



Infineon EGOLDradio is the key component

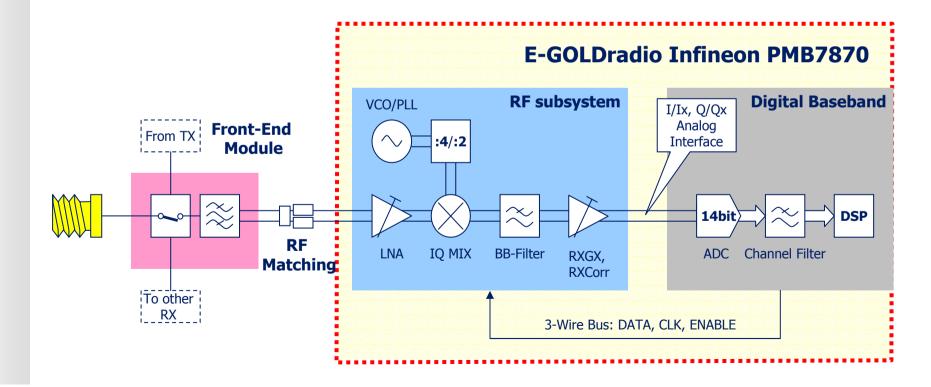


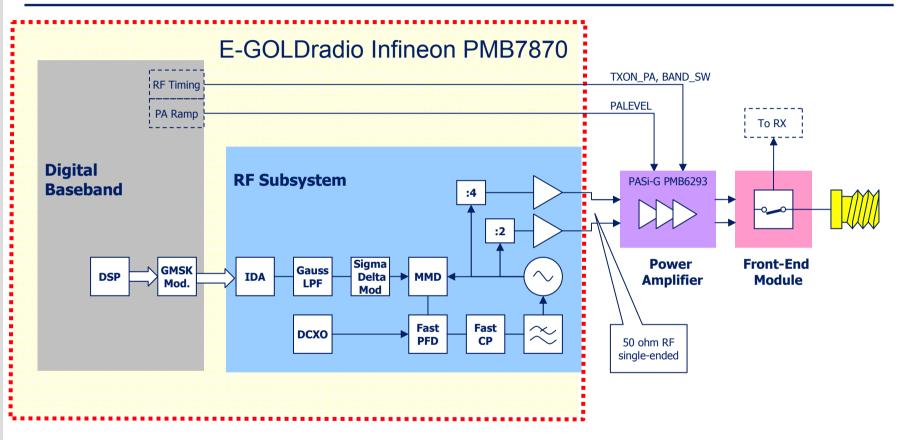
**Key component is:** Infineon **E-GOLDradio** PMB7870 GSM/GPRS Single Chip Solution that integrates Baseband System and Quad-Band GSM850/E-GSM/DCS/PCS RF Transceiver for voice and data applications

**Direct Conversion Receiver** is implemented by:

- Infineon EGOLDradio PMB787
- Epcos M081 Front-End Module

For each of the 4-band (GSM900, DCS1800, PCS1900 and GSM850), the RX path is mainly composed by similar functional blocks:



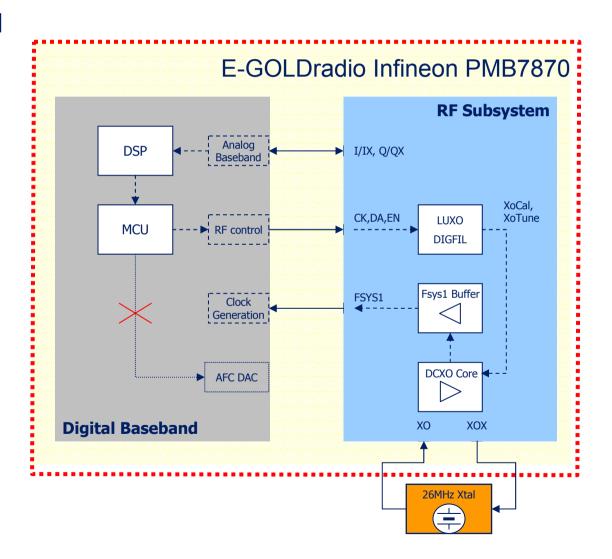


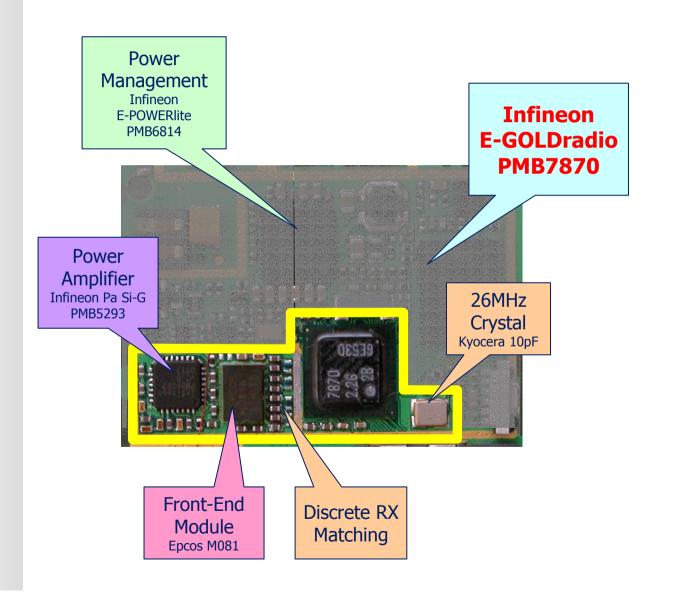
Sigma Delta Transmitter is implemented by:

- Infineon EGOLDradio PMB7870
- Infineon PMB6293 Power Amplifier
- Epcos M081 Front-End Module

## Digitally Controlled Crystal Oscillator

- Automatic Frequency Control loop is closed within EGR
- Only need external Crystal, no need for TCXO





Quad-Band Transceiver on Globe6:

**Components Placement** 



#### Infineon PMB7870 E-GOLDradio highlights

CMOS process

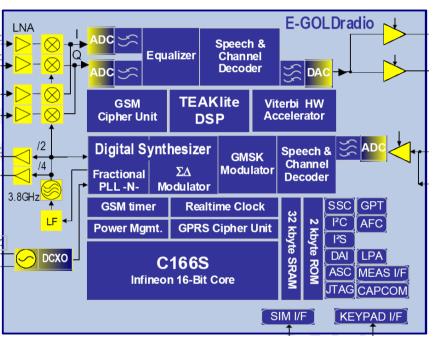


Low cost, high production capability

Very very Integrated



- Single ended outputs to PA
- integrated 3.8GHz VCO
- Integrated Loop filter
- 3 clock outputs
- Integrated Digitally Controlled Crystal Oscillator → no TCXO



#### Infineon PMB7870 E-GOLDradio highlights

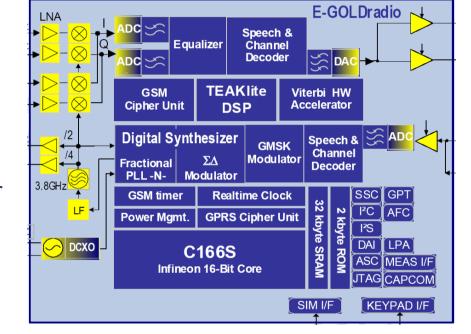
Integrated balanced LNAs for 850/900/1800/1900



■ Internal fractional-N  $\Sigma$ - $\Delta$  synthesizer



Delta-Sigma transmitter modulator



- Superior phase error performances than Quadtature Modulator
- Integrated enhanced resolution receiver
  - Constant Gain receiver

#### **Infineon PASi-G PMB6293**

- Quad-Band
- GPRS Class 12
- Integrated Closed Loop Power Control

Distribute Active Transformer



- Single-die 0.13 µm CMOS Technology
- Small Package 5mm x 5mm MLF
- 50Ω Input/Output Matching

#### **Epcos M081 Front-End Module**

- Quad Band Module
- MMIC Antenna Switch: low current consumption
- Two 2in1 RX SAW Band-Pass Filters

#### **RX Discrete RF Matching**

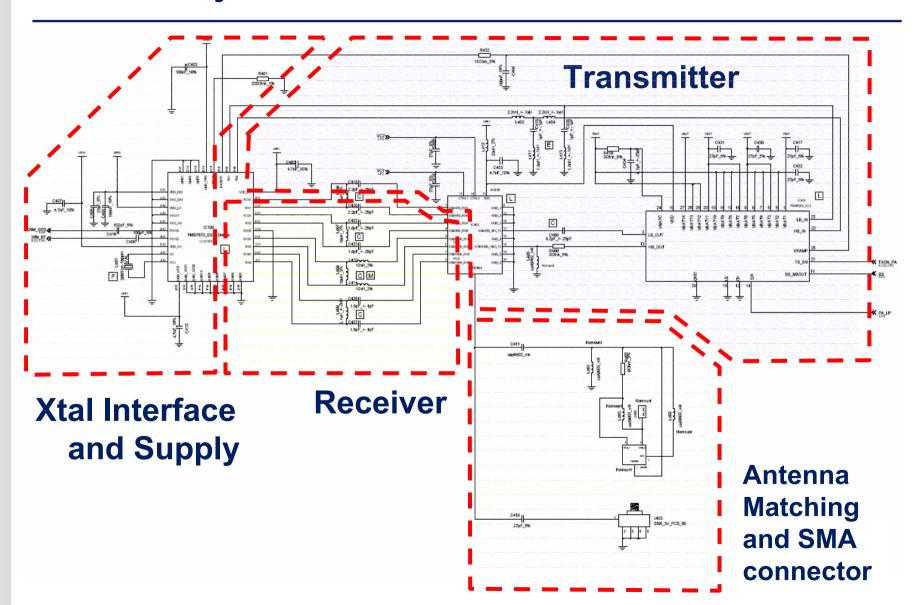
- 3 componets per band = 12 total passives
- Flexible implementation

#### **Kyocera 26MHz Crystal**

Cload = 10pF (mandatory for EGOLDradio)

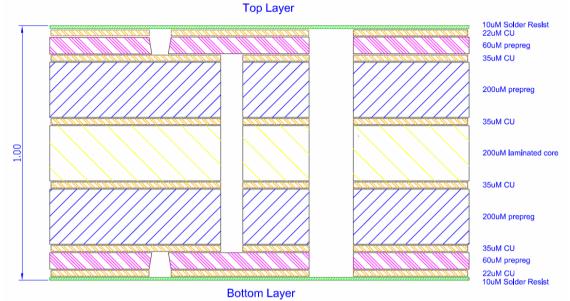
#### Quad-Band Transceiver on Globe6:

**Critical Components** 



#### **Board Lay-Up**

- 6-layers HDI
- external layer sequential build-up
- 75um width used for E-GOLDradio fan-out



#### Surface Finishing: Chemical Gold Plate Ni 5 uM / Au 0.1 uM

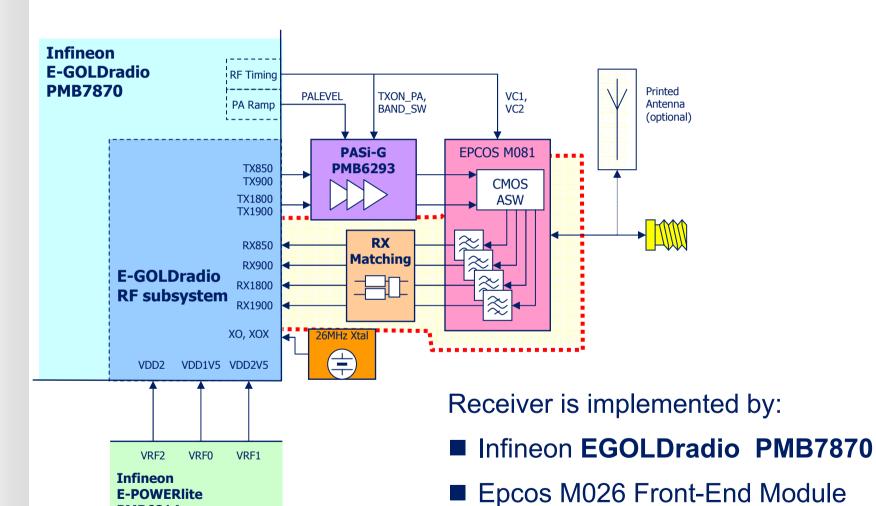
Design Clearance										
	Trace to Trace	Trace to Pad	Trace to Via	Via to Via	Via to Pad	Pad to Pad	Plane to Trace	Plane to Pad	Plane to Via	Plane to Plane
Layer 1	100um	100um	100um	100um	100um	200um	125um	150um	125um	150um
Layer 2	100um	100um	100um	100um	100um	200um	125um	150um	125um	150um
Layer 3	100um	100um	100um	100um	100um	200um	125um	150um	125um	150um
Layer 4	100um	100um	100um	100um	100um	200um	125um	150um	125um	150um
Layer 5	75um	75um	75um	100um	100um	200um	125um	150um	125um	150um
Layer 6	75um	75um	75um	100um	100um	200um	125um	150um	125um	150um

## **Globe6 RF System**

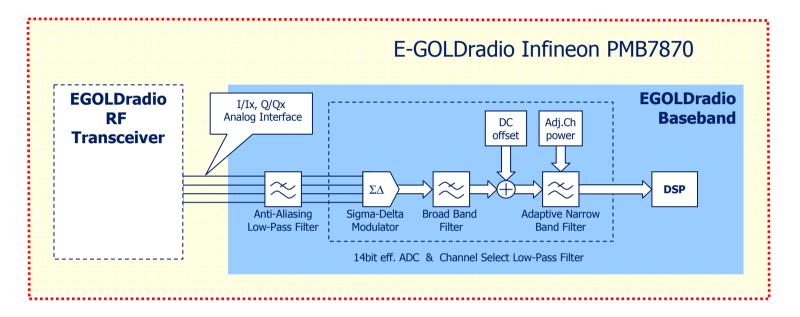
## Receiver

PMB6814

#### Globe6 RF System: Receiver



Discrete RX matching



#### Analog Pre-Filters:

1st order RC low pass filter as anti-aliasing pre-filter with a typical 3 dB attenuation @6MHz (enhanced mode). Note that I/IX and Q/QX for RX path are multiplexed together signals of the TX path

#### ■ Σ∆ Analog-to-Digital Converter and baseband filter

- 4th-order Sigma-Delta (ΣΔ) modulator and a subsequent digital decimating low pass filter performs the A/D conversion at a sampling rate of 26 MHz offers the required effective 14-bit resolution
- The samples are processed by a multi-stage low-pass filter for channel filtering. Depending on the level of adjacent channel interference, the last filter stage selects a filter with appropriate frequency transfer characteristic.

- The analysis follows the classical "RX-link-budget" approach:
  - the impact of the various functional blocks along the RX path, are summed up to the I/Q interface, where some condition required for the baseband correct functionality are verified.
- The design parameters will be usually:
  - the Signal-to-Noise Ratio (SNR) within the baseband channel select filter passband, where 8dB are assumed to be the minimum requirement
  - the Signal-to-Noise plus Distortion (co-channel interference) Ratio (S/N+I), same 8dB requirement as SNR.
  - the maximum input level that doesn't overdrive the baseband ADC, i.e. differential 2.0Vpp typ., 1.9Vpp min
- The analysis is first order approach, doesn't fully represent the platform limits, where fully compliant FTA and laboratory measurements should be regarded as reference.

#### **Conformance Requirements**

■ The receiver performances should fulfill specification

3GPP TS 05.05: "Radio transmission and reception"

Detailed testing procedure can be found in

3GPP TS 51.010-1: "Mobile Station (MS) conformance specification; Part 1: Conformance specification"

#### **RX** link-budget

- Reference Sensitivity (3GPP TS 51.010 Sub 14.2)
  - This performance is limited by the noise added by the receiver
  - Signal gain and noise figure are calculated through the receiver chain, and summed by classical Friis formulas to get the overall Noise Figure performances at baseband I/Q analog interface, where the noise introduced by ADC is also summed.
  - The Signal-to-Noise Ratio (SNR) at baseband I/Q interface must be greater than the minimum requirement form Baseband.
- Typical Sensitivity Performances for BP30-Globe6 are
  - -109dBm for GSM900 / GSM850
  - -108dBm for DCS1800 / PCS1900

#### Example from "BP30\_RX\_link\_budget.xls" (EGSM900)

Stage definitions		PCB loss	BPF	SMARTI-SD2				
					total gain	delta gain	corr. set	
actual gain	min	-0,40	-4,50	51,50	46,60	6,40 dB	0,0 dB	
· ·	wc corr gain			51,50	46,60			
	typ	-0,30	-3,70	57,00	53,00 R	ex target gain		
	max	-0,30	-3,70	62,50	58,50	-5,50 dB	0,0 dB	
	wc corr gain			62,50	58,50		•	
actual NF	max	0,40	4,50	3,70				
	typ	0,30	3,70	2,40				
	min	0,30	3,70	2,40				
Reference Sensitivity 3GPP TS 51.010 Sub 14.2					I/Q interface			
min gain case min gain, max IL passives, max NF								NO gain correcti

Reference Sensitivity 3GPP TS 51.010 Sub 14.2					I/Q interface		
min gain case	NF			NO gain correction			
cascaded gain [dB]		-0,40	-4,90	52,60		_	
cascaded NF [dB]		0,40	4,90	8,60			9,04 dB system NF
wanted signal [dBm]	-102	-102,40	-106,90	-49,40	0,76 mVrms	1,07 mVp	
noise level [dBm/Hz]	-173,98	-173,98	-173,98	-112,78	0,23 mVrms	513,60 nV/Hz	540,15 nV/Hz noise level w/ADC
SNR [dB]	18,97	18,57	14,07	10,37			9,93 dB baseband SNR
typ	typ gain, typ IL passives, typ NF						
cascaded gain [dB]		-0,30	-4,00	59,00		<u>.</u>	
cascaded NF [dB]		0,30	4,00	6,40			6,49 dB system NF
wanted signal [dBm]	-102	-102,30	-106,00	-43,00	1,58 mVrms	2,24 mVp	
noise level [dBm/Hz]	-173,98	-173,98	-173,98	-108,58	0,37 mVrms	832,96 nV/Hz	841,34 nV/Hz noise level w/ADC
SNR [dB]	18,97	18,67	14,97	12,57			12,48 dB baseband SNR
max gain case	max gain, min IL passives, min I	NF					NO gain correction
cascaded gain [dB]		-0,30	-4,00	64,50		_	
cascaded NF [dB]		0,30	4,00	6,40			6,42 dB system NF
wanted signal [dBm]	-102	-102,30	-106,00	-37,50	2,98 mVrms	4,22 mVp	
noise level [dBm/Hz]	-173,98	-173,98	-173,98	-103,08	0,70 mVrms	1569,00 nV/Hz	1573,47 nV/Hz noise level w/ADC
SNR [dB]	18,97	18,67	14,97	12,57			12,54 dB baseband SNR

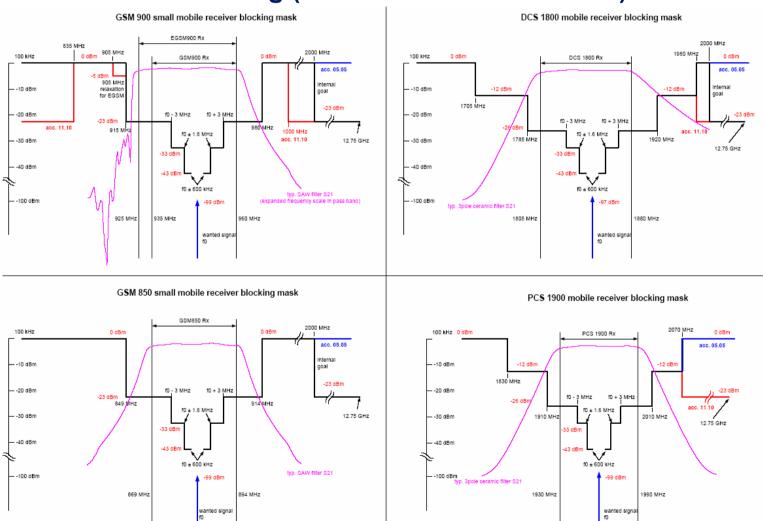
#### **RX** link-budget

- Adjacent channels rejection (3GPP TS 45.005 Sub 6.3)
  - Worst case is for levels according to GPRS requirements
  - The adjacent and alternate channels are supposed to be fully rejected by baseband digital channel filter before the demodulator
  - The analog section of receiver must guarantee that the signal at baseband input will be not high enough to saturate the ADC
  - Therefore the peak voltage level is monitored at I/Q interface, checking that it doesn't exceed the maximum allowable input range
  - The EGR Low-Pass Filter at output stage helps to fulfill the requirements
  - Desensitization Noise Figure must be used as worst case

#### **RX** link-budget

- In-band Blocking (3GPP TS 51.010 Sub 14.7)
  - Desensitization noise figure must be used
  - Typically the worst condition is for the 3MHz blocker.
  - For the case where the blocker frequency is N x 26MHz, a spurious
     response might be encountered, where EGR downconverts a fraction of input blocker power just superposed to baseband signal at I/Q interface.
  - The spurious response becomes Co-Channel Interference
  - The ETSI standard allows some exception with relaxed reqirements

#### Out-of-band Blocking (3GPP TS 51.010 Sub 14.7)



#### **RX** link-budget

- Out-of-band Blocking (3GPP TS 51.010 Sub 14.7)
  - The RF SAW BPF will greatly reject the disturbing signal
  - EGR spurious response at multiple of RX frequency shall be verified as well: at N x RX frequencies, it might occur that a blocker signal will be downconverted to baseband directly superposed to wanted signal, thus becoming Co-Channel Interference.
  - The signal at input of EGR is definitely no more differential: at 5.5GHz the signal from the BPF and matching is nearly common mode on the balanced input pins of RX port. Hence the common mode rejection is considered in the RX-link budget
  - The evaluation of rejection in the far blocking band is not easy, since parasitic phenomena appear at several GHz frequency, thus some assumption must be made or also simulations could be performed.

#### **RX** link-budget

- Max. Receiver input (3GPP TS 51.010 Sub 14.3)
  - This will impact the compression point of EGR receiver
  - EGR will be set in low-gain mode and therefore increased NF shall be accounted.
  - The SNR at I/Q interface shall be evaluated, as well as the resulting signal peak, in order to verify that baseband demodulator will have enough margin to operate with prescribed Nominal Error Rate and also that the ADC dynamic range will not be exceeded.

#### **RX** link-budget

- Intermodulation (3GPP TS 51.010 Sub 14.6)
  - The test condition stress the so-called 3rd-Order Intermodulation performances of the RF front-end, since the interferers frequencies are defined such that the 3-rd order intermodulation product will lie just superposed to useful signal, therefore becoming a co-channel interferer.

The classical formula to be used is:

#### PIM3@out [dBm] = 2 PA@in [dBm] + PB@in [dBm] - 2 IIP3 [dBm] + G [dB]

where PIM3 is the intermodulation product level at output of EGR, the IIP3 is the third-order input-referred intermodulation intercept point for EGR, PA and PB are the blocker level at input of EGR, and G is the gain for useful signal of EGR itself.

 At I/Q interface, the S/(N+I) shall be monitored in order to find if it exceed the wanted minimum level.

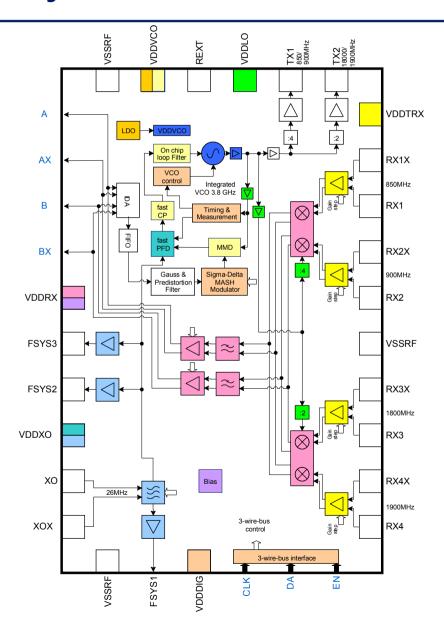
#### **RX** link-budget

- AM suppression (3GPP TS 51.010 Sub 14.8)
  - The even-order nonlinearity of the direct-conversion receiver will produce a DC contribution that will become superposed to downconverted signal at baseband output.
  - What can be expected is a DC step in the middle of the RX burst at the baseband interface, which level is estimated through the AM suppression figure started in the EGR specification, actually the ratio of the I/Q levels peak-to-peak to DC step.
  - Therefore that is the monitored parameter for this test case.

#### **RX** link-budget

#### Threshold behavior

- For the normal working functionality of the receiver, three main gain step are defined:
- 63dB gain for input level less than -90dBm
- 57dB for input level ranging from -93 dBm to -54dBm
- 22dB for input level above -57dBm
- Input ranges are overlapping because of hysteresis mechanism, which is implemented to limit the transitions between contiguous gain states for received signal at the edge of the ranges.
- In the limit conditions is useful to estimate the SNR at I/Q interface as well as the foreseen signal peak level, in order to verify that the target working condition for baseband demodulator will be fulfilled (with some margin) and signal peak will be not too high to run the risk of overloading the ADC range.



#### **RX** Active

RF Engine: RX mode

- Antenna Switch: connects the antenna to suitable RX/TX path
- RF SAW Band Pass Filters: reject out-of-band blocker signals
- **Discrete matching**:

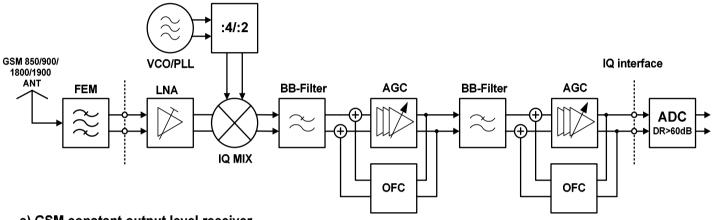
  Implement complexconjugate matching for LNA inputs
- RF Transceiver:

downconvert to baseband the In-phase and Quadrature component of received RF signal, amplified to match the dynamic range of baseband ADC

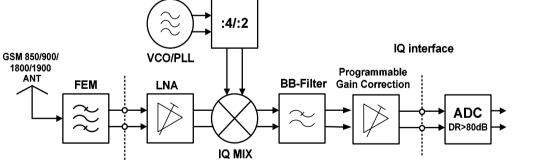
■ BB Processor:

Convert to digital domain the recieved I/Q signal, apply digital filter, equalize (Viterbi decoder) and extract several metric of received burst, other thandemodulated bitstream

#### **GSM Direct Conversion Receiver Principles – Block Diagram**



a) GSM constant output level receiver



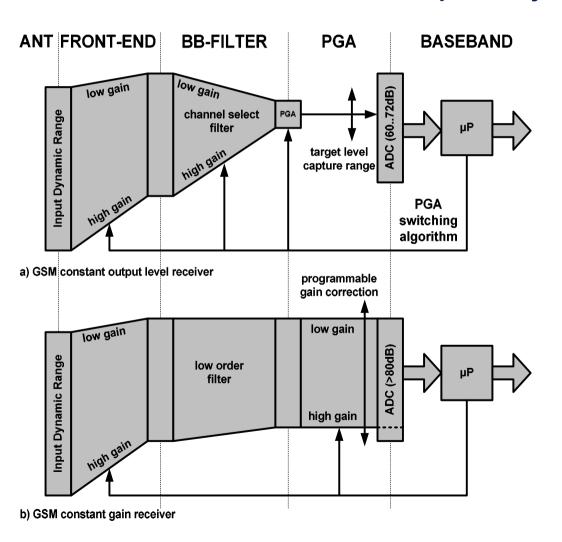
b) GSM constant gain receiver

Constant

**Gain RX** 

Concept

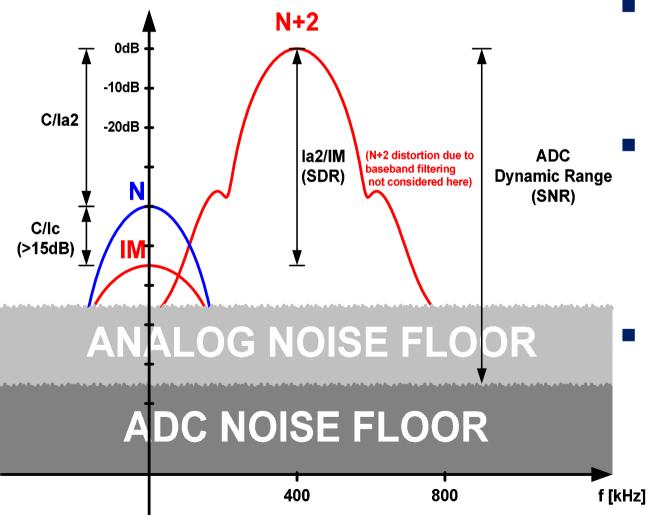
#### **GSM Direct Conversion Receiver Principles – Dynamic Range Flow**



- In constant IQ output level receiver the AGC algorithm running in the basebend keeps the level of I/Q within small range.
- But nowadays the BB ADC exibiths a very wide input level
- With Constant gain receiver the goal is to take advantage of such high dynamic range to get simpler gain implementation and simplified hardware.

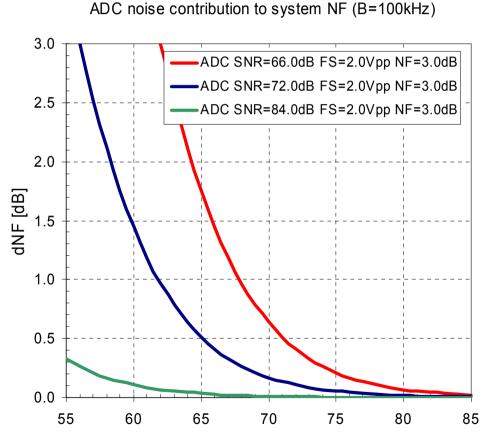
#### signal to distortion ratio (SDR) requirements @ N+/-2 interference

(GSM 45.005: C/la2max = - 43dB)



- The gain setting applies for both wanted signal and adjacent channels, e.g. N+/-2 Interf.
- The gain should be high enough that wanted signal at I/Q interface should be high enough to overcome the ADC and Analog noise floor
- But the gain should not be so high that the faded Adjacent channel N+/-2 will result high enough to overdrive the ADC

#### **ADC Noise Contribution to System Noise Figure vs. RX Gain**



RX Gain [dB]

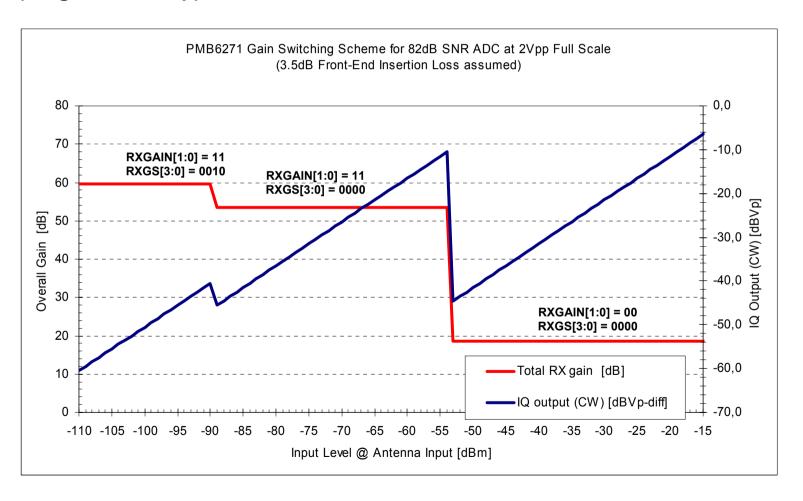
- typical ADC SNR (B=100kHz)
- typical RX noise figure (NF→IC)
- typical systematic noise contribution depending on RX Gain
- → degradation with ADC SNR=82dB nearly 0.3 dB at NF=3.0dB
- → means that with E-GOLDradio's internal ADC the loss of sensitivity performances with RF Noise Figure = 3dB is only 0.3dB with RF Gain around 60dB

### **RX Gain Setting**

#### Threshold behavior

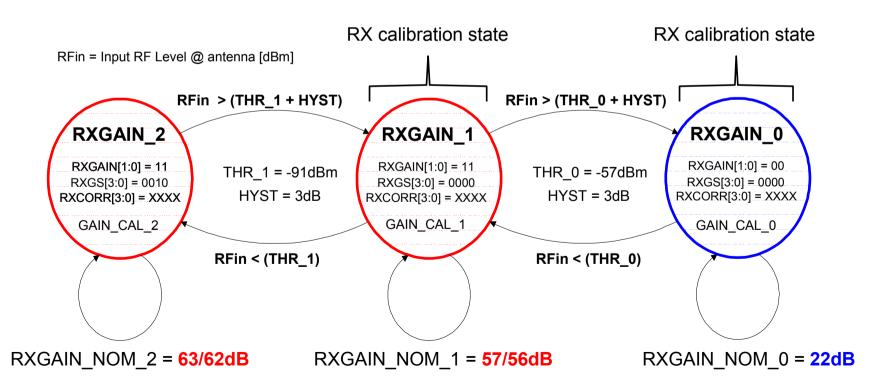
- For the normal working functionality of the receiver, three main gain step are defined for E-GOLDradio RF subsystem Setting:
  - 63dB gain for input level less than e.g. -88dBm
  - 57dB for input level ranging from e.g. -91 dBm to -54dBm
  - 22dB for input level above e.g. -57dBm
- Input ranges are overlapping because of hysteresis mechanism, implemented to limit the transitions between contiguous gain states for received signal at the edge of the ranges.
- The Software doesn't differentiate the different gain performances for Low/High band, that are handled through calibration
- RXCORR = -6..+6dB correction range in 1dB step for RX calibration

■ Gain Switching Scheme Example for 82dB SNR ADC at 2Vpp Full Scale (Single Gain Step) → used for E-GOLDlite + SMARTi-SD2 and E-GOLDradio



### **RX Gain Setting**

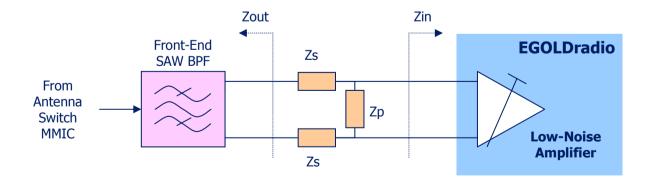
- The SW implementation of RX gain algorithm is basically a state machine
- For baseband ADC with SNR = 82dB at 2Vpp Full Scale
  - → Single Step Scheme and only a 2-Point-Calibration



### **RX Matching**

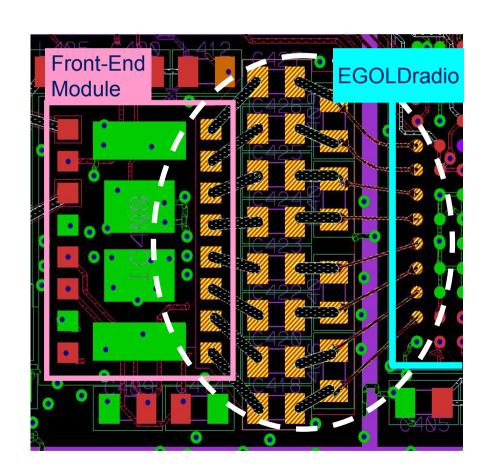
- Target is to transform FEM output impedance to complex conjugate of EGOLDradio input impedance
  - Minimize mismatch loss → Maximize sensitivity performances
  - Also impact RX blocking performances

3 components per band = 12 total passive



### **RX Matching**

- Simulation starts from s2p parameter of EGR and FEM
- Should include effect of layout
- Otherwhise: complex differential measurement on real board
- Provides first approximation, then fine tuning and verification by measurements of BER performances



#### **Calibration**

- For each used status of RXGAIN[1:0] (basically related to LNA gain setting) a separated correction factor should be used
- The RXGS[3:0] and RXCORR[3:0] are high precision gain stages and don't need extra calibration



Only two different calibration-correction factor are used

- Actually in SW (eep) there is no temperature and channel compensation default
- Should be defined on Customer board based on some statistics

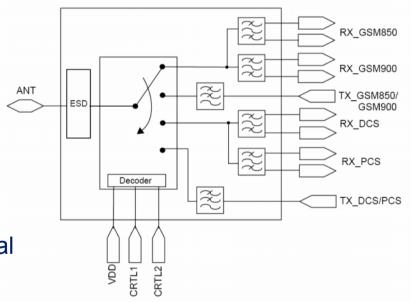
#### **Calibration**

- Taking advantage of RXCORR[3:0] availability, the calibration factors are used to build different RXTX register programming, i.e. different RF Gain setting
- This is different from other previous platforms where the RX gain correction algorithms was algebraically sum the correction factors for RXLEV-channel-temperature on the read-out from DSP, with no changes in the RF Gain configuration.
- With E-GOLDradio the approach is the opposite: the algebraically sum the correction factors for Gain status-channel-temperature is used to program different RF Gain, in order to get correct evaluation of DSP reading, which doesn't need any more compensation

## **Globe6 RF System: Front-End Module**

### **Epcos FEM M081**

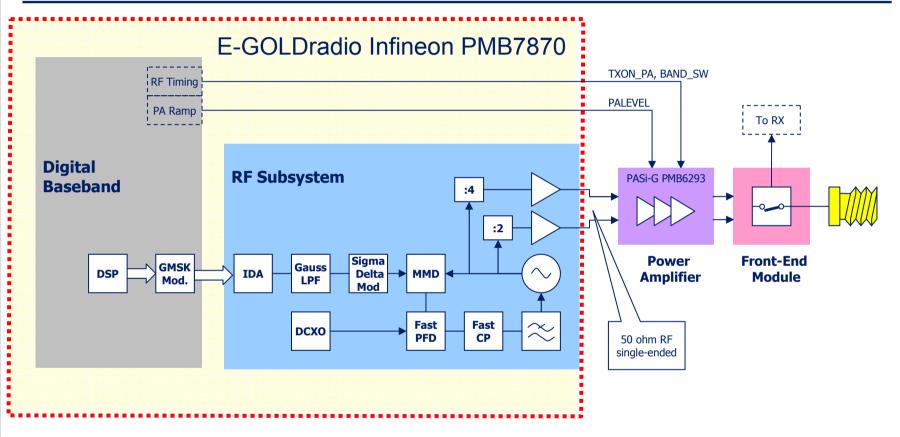
- Quad Band Module (5.4 x 4.0 mm)
- MMIC SP4T RF switch
- 2 x 2in1 RX SAW Band-Pass Filters
- Driven directly by E-GOLDradio TOUT pads
- Mimumum current consumption
- Doen't needs any special layout typical of custom FEM with complexed integrated matching



Switch Mode	CTRL1	CTRL2
GSM1800/GSM 1900 RX	High	Low
GSM850/GSM900 RX	Low	Low
GSM850/GSM900 TX	Low	High
GSM1800/GSM1900 TX	High	High

## **Globe6 RF System**

# **Transmitter**



Sigma Delta Transmitter is implemented by:

- Infineon EGOLDradio PMB7870
- Infineon PMB6293 Power Amplifier
- Epcos M081 Front-End Module

**RF Engine: TX mode** 

#### BB Processor:

provides bitstream, programs RF transceiver, generates timing signals to Power Amplifier and Antenna Switch, generates analog PA ramping signals

#### RF Transceiver:

modulates the baseband info and upconverts to RF

#### **■ Power Amplifier**:

amplifies weak RF signal from Transceiver up to Watt range, according to Power control signal from Baseband processor

#### ■ Antenna Switch:

connects the antenna to suitable RX/TX path, but also provides low pass function for TX signal and its insertion loss limits somehow the unavoidable effect of antenna mismatch at power amplifier output

#### Discrete matching:

typically between PA and Antenna Switch there are some passive components for matching purposes (initially dummy 0ohm resistor). Also before antenna some matching components are usually placed

- First analysis performed is classical "TX-level-plan":
  - The components performances stated within datasheets are combined to verify the TX chain is able to fulfill the ETSI specifications.
- The parameters verified are:
  - maximum output power
  - harmonics
  - TX noise in RX band

■ See Excel sheet "Globe6\_TXlevelplan.xls"

### **Spurious Classification (Internal)**

- Depend on SD-family concept, were internally classified :
- Alpha
  - Spurious sidebands on the TX output signals when TX frequency is close to a multiple of the reference frequency (26 MHz):

$$f_{offset} = \pm (f_{TX} - (n * 26MHz))$$

- It can be seen that with PRBS modulation the spurious sideband which is at a multiple of 26 MHz still is a single line while the sideband on the opposite side of the TX carrier is spread.
- Typically the critical item is the 400kHz modulation spectrum at ± 2 ARFCN from 26MHz multiple,
  - GSM900.... 26MHz\*36 = 910MHz = ch100 → check ch98 and ch102
  - DCS1800... 26MHz\*66 = 1716MHz =  $ch541 \rightarrow check ch539$  and ch543
- Alpha spurs depends on PCB layout

### **Spurious Classification (Internal)**

#### Beta

- Spurious sidebands on the TX output signals when VCO frequency is close to a multiple of 13 MHz spurious
- The offset frequency of these sidebands is the frequency difference between the VCO/LO signal and a harmonic of half of the reference frequency.

$$f_{offset} = \pm (4 f_{TX} - (n * 13MHz))$$
 for GSM850 / GSM900  $f_{offset} = \pm (2 f_{TX} - (n * 13MHz))$  for DCS1800 / PCS1900

- Again, the critical item is the 400kHz modulation spectrum
- Beta spurs depends on PCB layout

### **Spurious Classification (Internal)**

#### Gamma

Spurious sidebands on the TX output signals which have an offset of multiples
of the reference frequency to the LO frequency.

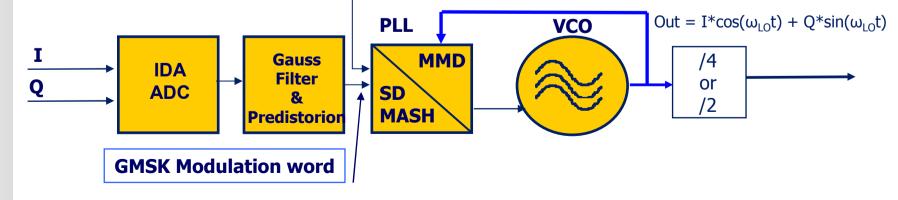
$$f_{offset} = \pm (n * 26MHz)$$

- The internal digital noise of EGOLDradio is the main spurious source
- Because of this, most of the bypass capacitor are in the nF range. (e.g. 100nF on VDD3, that is supply for digital section)
- They cause TX spurious in RX band
- On EGOLDradio there are Gamma-spurs in RX band
  - max 1 exception for Low Band
  - max 3 exception for High Band

"Analogue linear" GMSK Modulator TX concept like SMARTi DC+ **Channel word** VCO Out =  $I*cos(\omega_{10}t) + Q*sin(\omega_{10}t)$ LO or PLL Drive Q

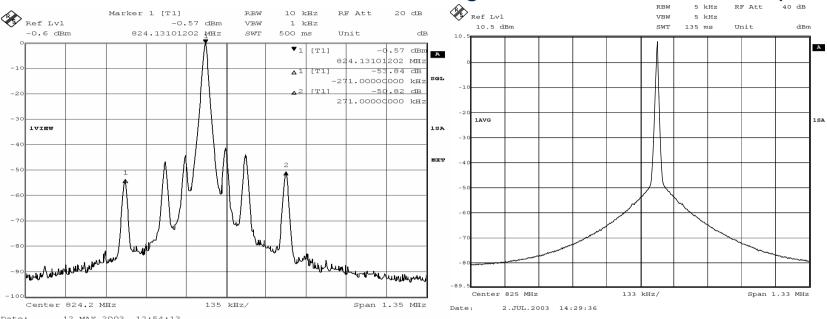
**Channel word** 

"Digital nonlinear" SD Modulator TX concept like SMARTi SD2



#### **Direct Modulator**

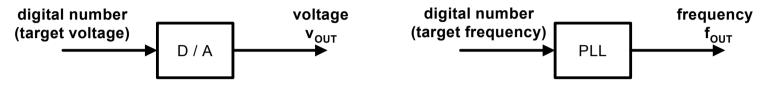
### Sigma-Delta Modulation Loop

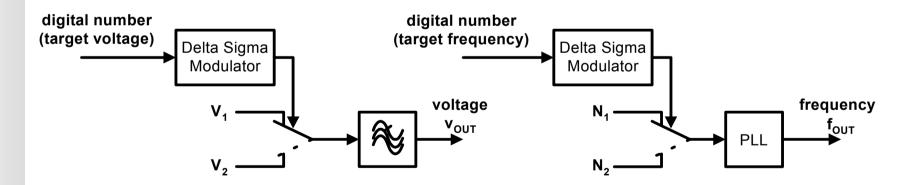


A Direct Modulator like SmartiDC+ needs a H3 filter, due to the sensitivity of leakage back to the Modulator and it needs a driver, due to linearity.

A Sigma-Delta Modulator is OK as it is.

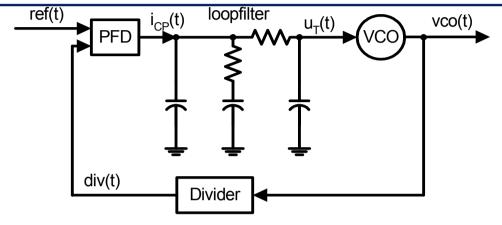
### Equivalence between DAC and PLL:





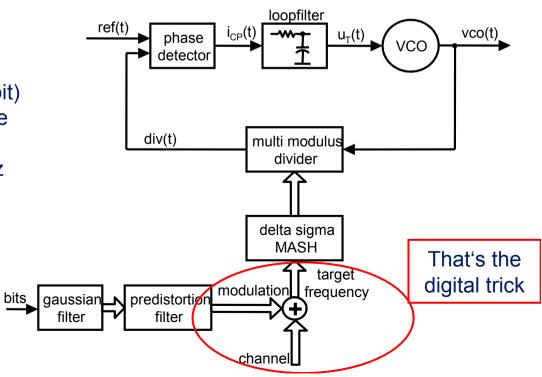
Now one can apply the ,tricks' known from DAC-design in PLL design. Therefore it is possible to decouple the frequency resolution from the loop multiplication!

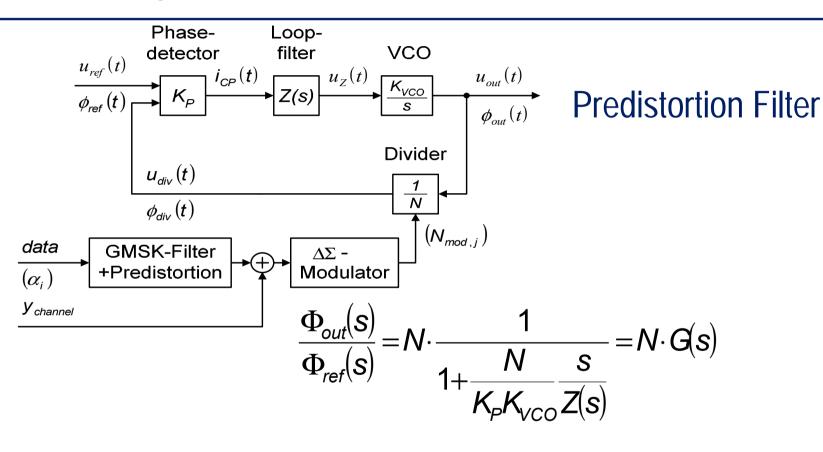
### **Integer-N architecture**



#### Frac. N architecture

- 3Hz frequency resolution (23bit)
- -90dBc/Hz inband phase noise
- 25 dB attenuation @ 400 kHz
- 140 dB attenuation @ 20 MHz
- <3° phi<sub>rms</sub>





$$f_{out}(s) = N_{mod}(s) \cdot f_{ref} \cdot G(s) \cdot G(s)^{-1} = N_{mod}(s) \cdot f_{ref}$$

→ Modulation error improved by using digital predistortion in conjunction with "OLGA"

### **Power Amplifier in Complete System**

#### **New problems**

#### Output Power:

is reduced by Insertion Loss of Antenna Switch, etc.

Frequency response must be equalized in HW (discrete matching) or in SW

#### ■ Harmonics:

May leaks to other PCB srtucture (e.g. the VBAT up to battery pack) and irradiate

### ■ Timing:

provided by baseband, to be defined in SW

#### **■ EGR** phase error:

The (variation of) backward power from PA input at VCO frequency might impact the modulation performances

#### Relaxations

#### **■** Harmonics:

mitigated by Antenna Switch Low-Pass function

#### ■ Power Amplifier termination:

at least the insertion loss of Antenna Switch provides some limit of mismatch condition at PA output

#### **Baseband Interface**

#### 3Wire bus to RF Transceiver

- used to programm frequency, gain, and other setting and triggers the RF output
- several strobe (EN) free

#### Dedicated TOUT pads for "Trigger Outputs" digital signal

- easy link to GSM timer unit
- provide some mA
- used for TXONPA, and controls signals for Antenna Switch (+ LOW\_POWER mode for CmosPA)

#### Power Ramping

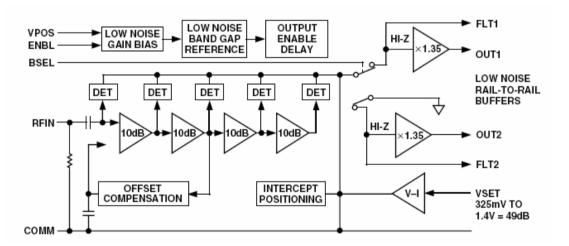
- triggered by GSM timer unit
- 11bit DAC with interpolator and low-pass filter

### **Output Power**

- Measured in 50ohm load, VBAT = 3.8V
- Maximum (usable) output power must be greater than target levels used in calibration, otherwise the board will be rejected in production test, i.e.:
  - 32.2 dBm for GSM850 and GSM900
  - 29.2 dBm for DCS1800 and PCS1900
- From project design perspective, controlled output power is expected to be at least equal to ETSI nominal power for maximum power level, i.e. :
  - 33 dBm for GSM850 and GSM900
  - 30 dBm for DCS1800 and PCS1900
- "Nice to have" margin of 1dB for maximum output power
- The Minimum VBAT can be considered 3.3V, Maximum Temperature +55°C
- In Extreme condition the output power can be reduced, but should not produce unwanted effects, e.g. switching spectrum rising

#### **Power Control**

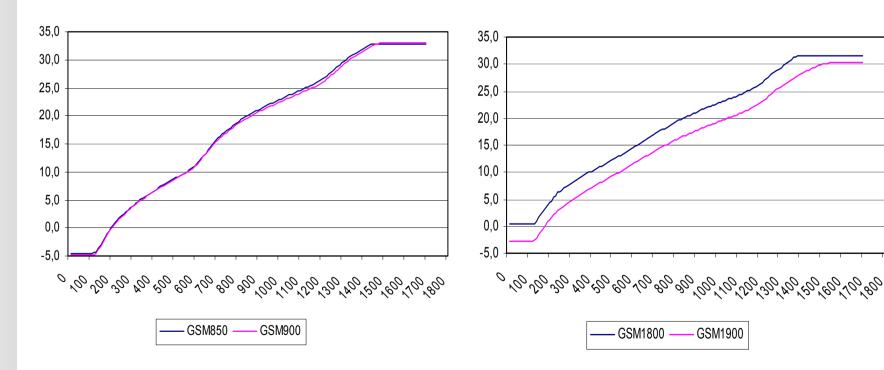
Logarithmic control is similar to other implementation on the market, e.g.

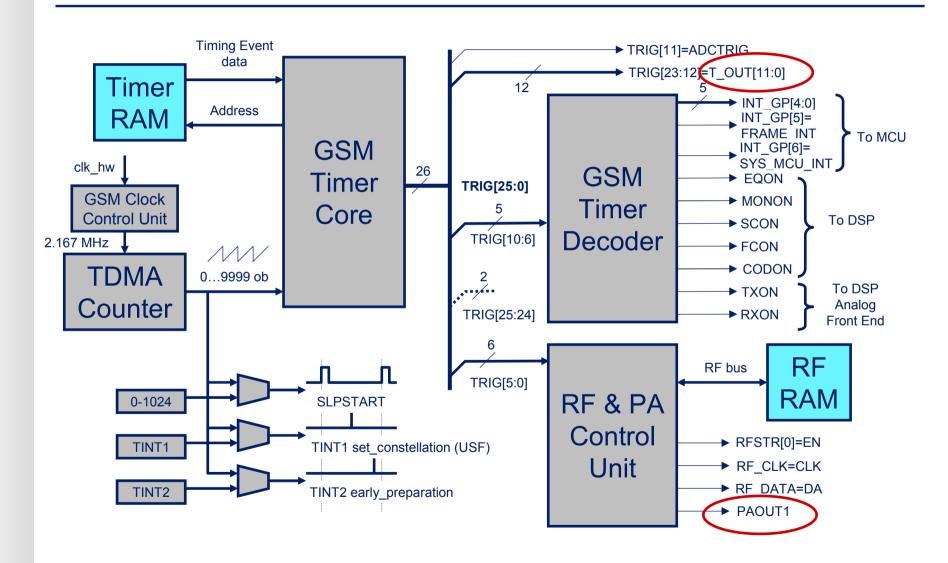


■ Typically such established controllers exhibit almost 50dB of control range, with excellent performances also in low power ranges

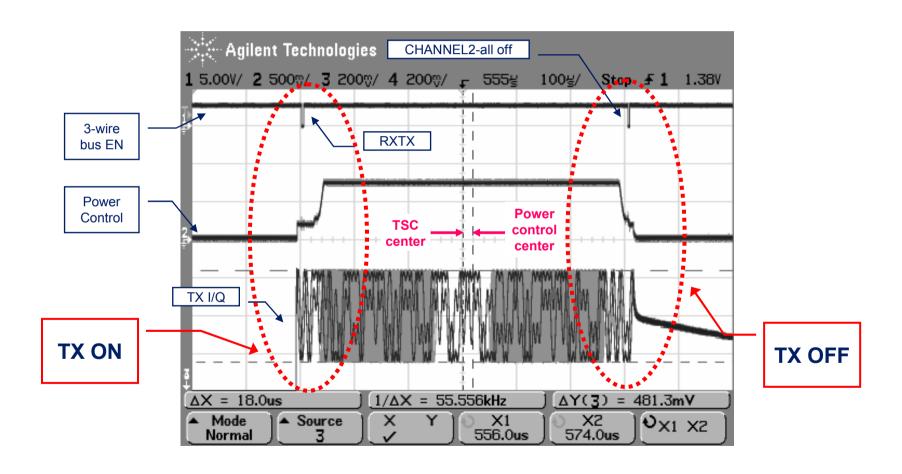
### **Power Control**

### Example of control characteristic



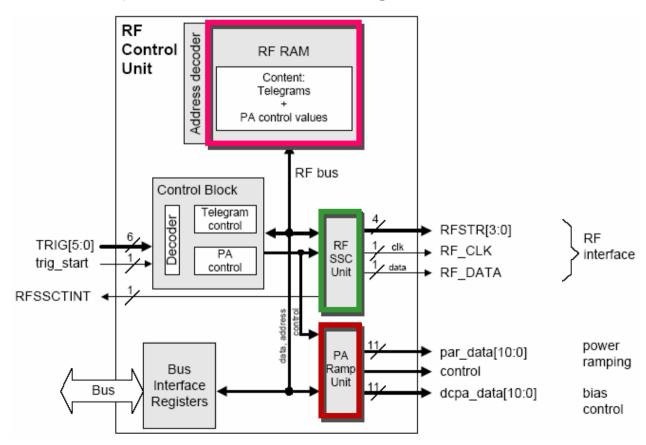


#### **TX Slot scenario**

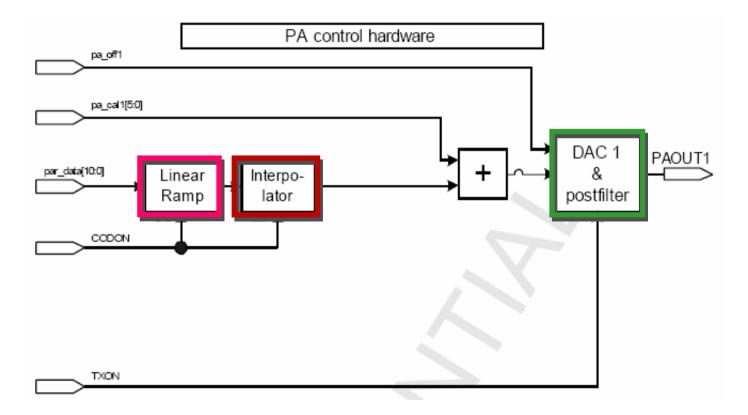


Main Sub blocks: Control Block, RF RAM, RF SSC Unit,

PA Ramp Unit, Bus Interface Register.



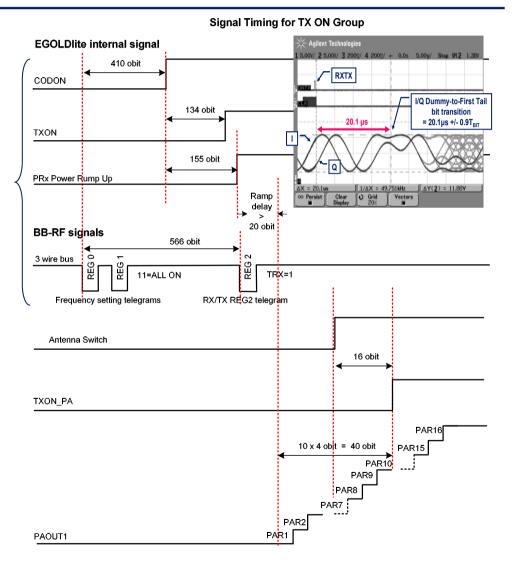
Main Sub blocks: Control Block, RF RAM, RF SSC Unit, PA Ramp Unit, Bus Interface Register.



### **TX ON sequence**

Internal Signals

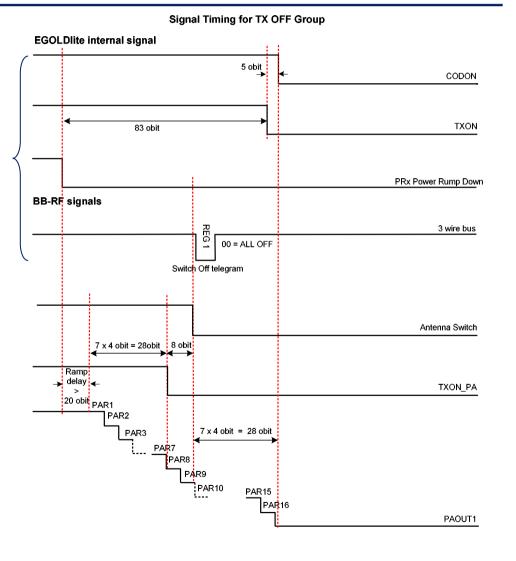
- 1. RXTX trigger RF
- 2. Antenna Switch
- 3. Ramp-up (last 6+1 used)
- 4. TXON PA



### **TX OFF sequence**

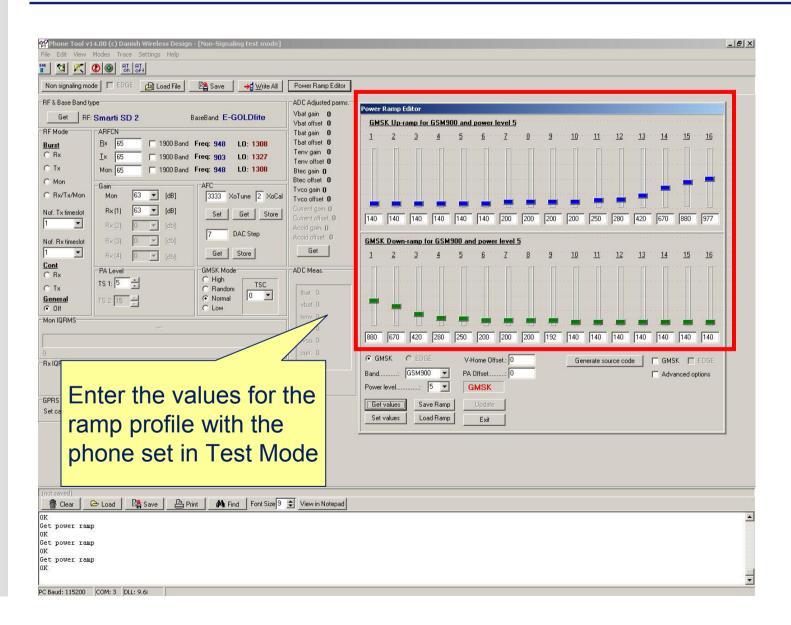
Internal Signals

- 1. Ramp-down (first 5 used)
- 2. TXON PA
- 3. Antenna Switch
- 4. RXTX all-off RF



### **Power ramp**

- The DAC values for ramp are stored in SW tables inside the source
- The Ramp signal is made of three sub sections,
  - initial ramp-up (1..15 values )
  - hold value (16-th entry)
  - and ramp-down ending part (1..16 values)
- Only a subset of ramp-up and ramp-down has effect on real power ramp
- To test the performances for the transmitter, the ramping profiles can be entered in the Phone Tool apposite menu for each power level
- The shape for the VRAMP signal is responsible for the resulting switching spectrum performance



### **Power Ramping and Calibration (in IFX software)**

- 6x11bit value are used to shape the ramp-up profile, 5x11bit for ramp-down
- One set of default ramps for each BAND, one default ramp for each PL
- The 16th value of ramp-up define the "Hold" level during the useful part of the burst.
- Compensation / calibration apply only to "Hold" value
- The finally used value is the resulting value from default level value plus compensation values (one for each PL)
- For the maximum PL, also correction is applied according to
  - Frequency: constant correction for each sub-band
  - Temperature: constant correction in each temperature sub-range
  - Battery Voltage: linear correction below Threshold, in 100mV step

frequency sub-bands			
GSM850	EGSM900	GSM1800	PCS1900
128 to 152	0 to 25	512 to 600	512 to 600
153 to 226	26 to 99	601 to 700	601 to 700
226 to 251	100 to 124	701 to 800	701 to 800
-	975 to 1023	801 to 885	801 to 885

Temperature sub-ranges [°C]	
-30 to −11	
-10 to +9	
+10 to +29	
+30 to +49	
+50 to +69	

#### **Calibration**

- Actual calibration performs measurements on each power level to find the calibration factor (applied only on power ramp hold value)
- The routine makes linear interpolation in case of reduced power measurements points (e.g. 3-point calibration)
- This is maybe not the best characteristic to be used, probably a quadratic function of linear power will give better results

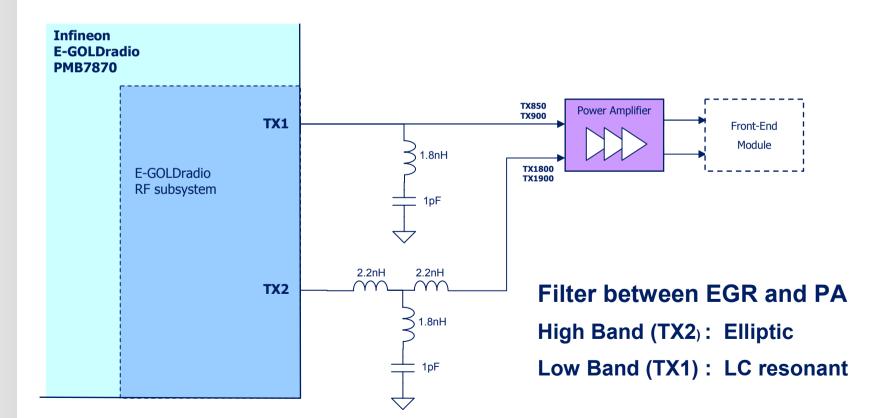
#### Remark:

- Actually in SW (eep) there is no temperature and channel compensation default
- Should be defined on Customer board based on some statistics.

### **Globe6 RF System: Transmitter**

### EGR peak phase error

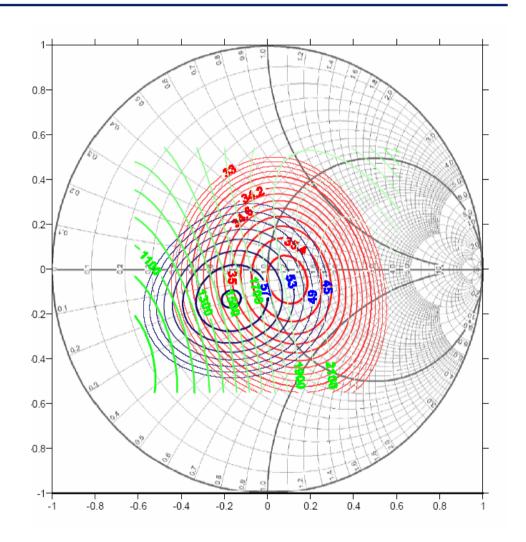
- The (variation of) backward power from PA input at VCO frequency might impact the modulation performances
- Some 3.8GHz filters are placed before PA in EGR application



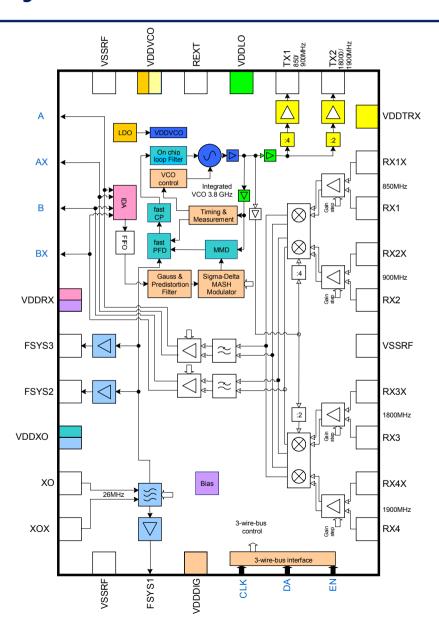
### **Globe6 RF System: Transmitter**

### **Load Pull Data**

- Shows how sensitive is the application to load variation
- The Output Power (red curves),
  PAE (blue curves) and Battery
  Current (green curve) are shown
  in the same Smith Chart at a fixed
  frequency (in this case 900 Mhz)
- If available at different frequencies, might be used to define the (optional) output matching



# **Globe6 RF System: Transmitter**



# **TX Active**

# **Globe6 RF System**

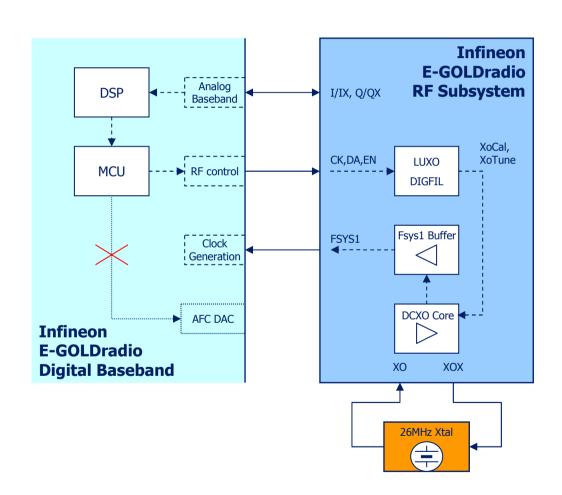
Mod. M03-N7 / Rev. 2 BH02.HW.PP.000006

**DCXO** 

### **Digitally Controlled XO:**

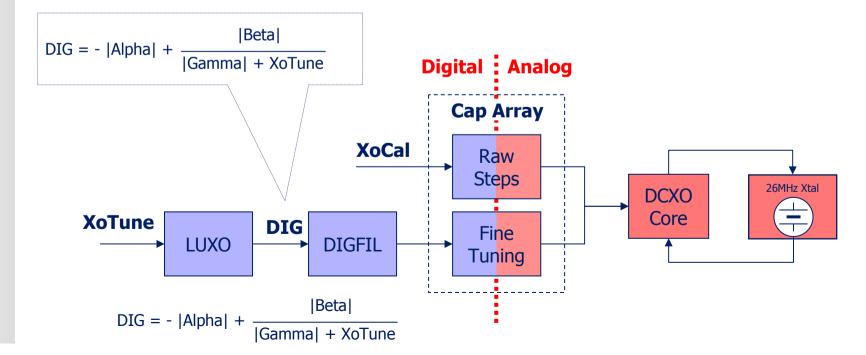
### **AFC** loop

- Automatic Frequency Control loop is no longer using analog AFC DAC
- Instead the updated AFC value is sent through the internal bus bus (XoTune)
- The AFC routine remains unchanged
- AFC value is scaled from 11-bit to 13-bit (0..8191)



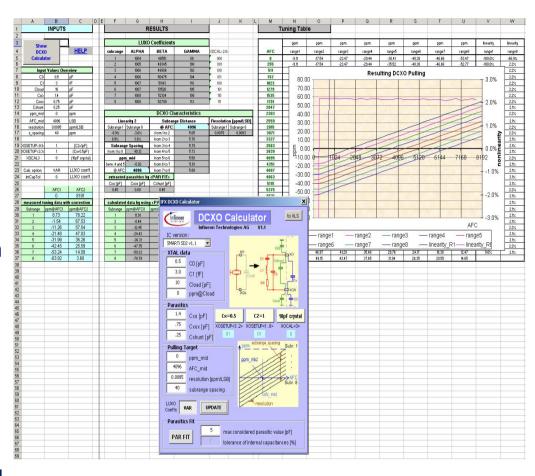
### **LUXO Coefficients**

- With Xtal Oscillator Linearization Unit LUXO enabled (default & recommended) E-GOLDradio elaborates internally the XoTune setting in order to achieve a linear tuning characteristics for DCXO
- The linearization depends upon Alpha-Beta-Gamma parameters



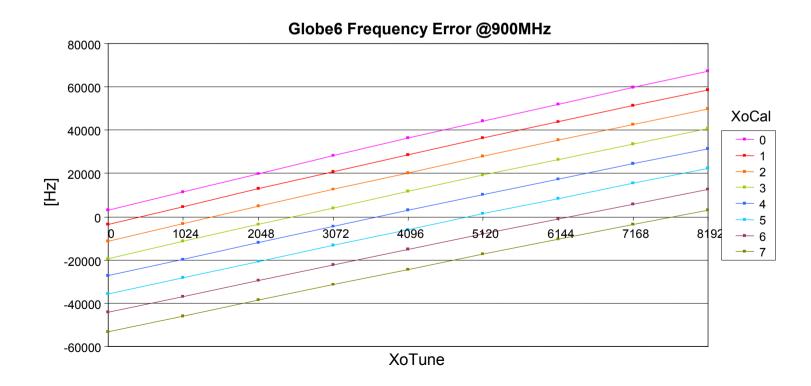
### **LUXO Coefficients**

- Alpha-Beta-Gamma are different for different crystals
- "DCXO\_Calculator.xls" is available form Infineon-RF Team to calculate LUXO coefficients for other crystal with compatible characteristics
- PCB parassitic has some impact on DCXO performance
- When implementing new Xtal or new PCB, should be verified:
  - The Frequency vs. XoTune and XoCal characteristcs: should be linear, equispaced and centered
  - The WakeUp time of DCXO: amplitude steady state should be reached in approx. 2-4ms



### **LUXO Coefficients**

- Several Subranges are available, to compensate Xtal variation
- DCXO Tuning characteristic is very linear



### **Temperature Effect**

- By changing the temperature the Xtal, thus all the overall DCXO, changes its output frequency
- The DCXO is more sensitive than TCXO, being the latest a "Temperature Compensated XO"

### Therefore:

- During normal call, the AFC update should be fast enough to compensate the temperature change at board level due to self-heating at different Power Levels
- At cool boot of the board, the ppm variation of 26MHz master clock should be within the limit of the capture range of FCB by DSP algorithm
- Since the environmental temperature produces 26MHz variation in terms of "ppm", the worst case is for a BCCH at PCS ch 810 (max RX channel, with same ppm → max frequency error at IQ interface)
- Some temperature compensation routine might improve this performances (not yet implemented)

### **Calibration**

- Production calibration need extra step to find the best XoCal range
- This should be done as first step
  - Measure frequency error Fmax at XoCal=0 XoTune=4096
  - Measure frequency error Fmin at XoCal=7 XoTune=4096
  - Compute the subrange spacing by (Fmax-Fmin) / 7 (this supposes that subranges are equally spaced), then find the subranges that gives the minimum frequency error for XoTune=4096 setting

```
XoCal = round [ (Fmax * 7) / (Fmax - Fmin)]
```

- Then find the XoTune setting which nulls the error frequency at chosen XoCal subrange
- This should be done as previous TCXO calibration

### **26MHz Crystal Requirement**

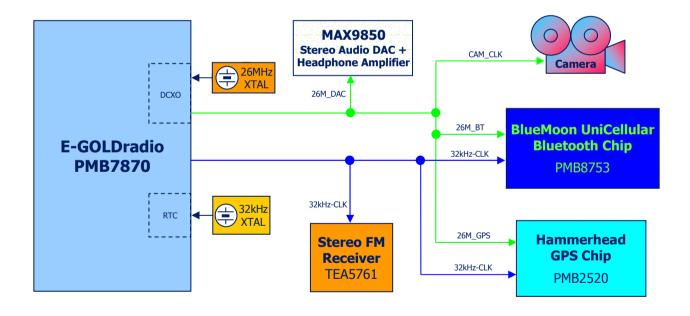
Crystal parameters from EGR datasheet:

Nominal Load Capacitance	C <sub>LOAD</sub>		10		pF
Motional Capacitance	C1 <sub>10pF</sub>	5.3	6.6	7.9	fF
Shunt Capacitance	C0 <sub>10pF</sub>	1.3	1.6	1.9	pF

- Kinseki Kyocera KSX-23-26000KAA-GA0 is default Xtal on Globe6
- For EGOLDradio application, Cload = 10pF is mandatory

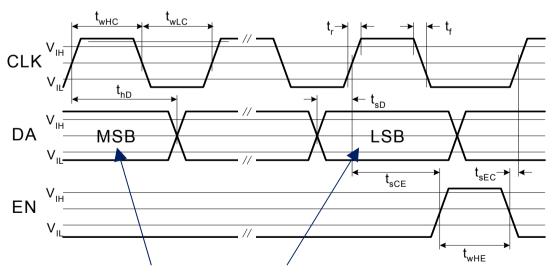
### Clock usage on Globe6

- 26MHz master clock from DCXO
- 32kHz from Real Time Clock



# RF Register Setting

- The 3-wire bus is used to transmit the 24-bits telegrams, which are necessary to program the SD2 internal control registers
  - The bus consists of three signals: CLOCK, DATA, ENABLE
  - DATA are latched within SD2 at rising end of CLK signal
  - Rising edge of ENABLE means that register transmission is complited (then ENABLE can stay high up to next register transmission)



MSB first, LSB last: On oscilloscope the "Address" should be read from the end of transmitted data in reverse order

- Register setting can be divided in two groups depending on their usage:
- "Initialization" registers
  - Used to initialize the EGOLDradio RF internal settings at every power-on (i.e. every time VDD1V5 supply is applied)
- "Burst Activity" registers
  - Used to set frequency, gain, etc and to start RX and TX activity

 Please refer to EGOLDradio datasheets for exact definition of Registers bits meaning

### "Initialization" Registers

- XO\_Init1, XO\_Init2, XO\_Init3: select the 8-10pF Xtal mode, initialize the Linearization Unit (LUXO) for DCXO and set the FSYS output buffer usage
- XO\_Tune: fine tune the DCXO 26MHz master frequency, thus achieving tuning of RF local oscillator frequency (used for AFC algorithm)
- Init registers: sets other internal setting of EGOLDradio

### **XO\_InitX** Registers

- All XO\_Init to be sent once after EGOLDradio Power-up
- Required recalculation of XO\_Init registers according to XO\_Cal setting, possibly needed in production line.
  - Alpha, Beta, Gamma to be provided by Infineon according to the 26MHz Xtal characteristics
  - XO\_Init telegrams recalculated at power-up according to XO\_Cal value, stored in the flash sector together with RF calibration parameters.
- Any Init word telegram should be sent after power-up, following XO\_Init, so it is suggested to handle them in the same way of XO\_Init registers programming.

### **XO\_Tune Register**

- XO\_Tune to be handled in the same way of AFC DAC register in conventional code:
  - every time the AFC register is changed by GSM software running on the Mobile, an updated XO\_Tune register must be sent to EGOLDradio
- The more frequently XO\_Tune is updated, the lower frequency error during GSM call, because 26MHz variation due to change of Xtal temperature are more frequently corrected
- Since Xtal oscillator is more sensitive to temperature variation than VC-TCXO, the platform is obviously more sensitive to temperature variation → should be compensated in SW

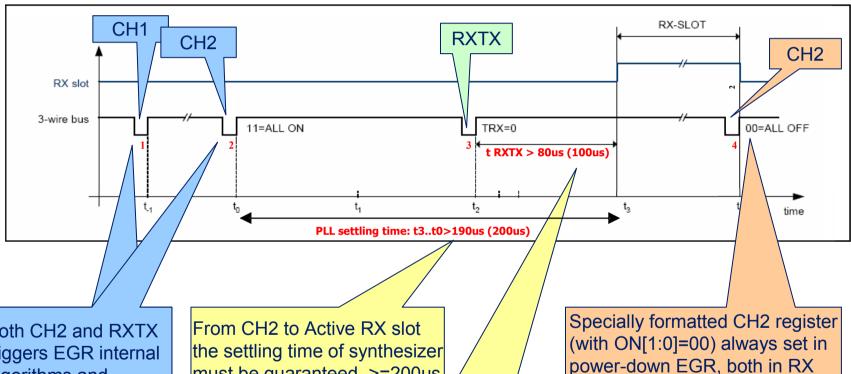
### "Burst Activity" Registers

- CHANNEL1 (REG0) and CHANNEL2 register (REG1) :
  - used to set the RX-TX frequency and band
  - Specially formatted CHANNEL2 register (with ON[1:0]=00) always set in power-down RF transceiver, both in RX and TX modes
- RXTX Register (REG2):
  - set the RX gain and RX common mode DC levels
- For each burst (or sequence of burst with same frequency) there will be always CH1 and CH2, then RXTX, then OFF register programming → total 4 registers

### **Frequency Setting Registers**

- Given the GSM ARFCN channel, the standard (e.g. 45.005) explains how to map it to the TX-RX carrier frequency
- Once the Carrier frequency, Fo, is known, the Fvco frequency is simply 4x Fo for GSM900/850 or 2x Fo for GSM1800/1900
- The INTEGER channel word (CH7..CH0) is
  - integer part NI = floor(Fvco/26MHz), basically it is the "floor" number of time is needed to multiply 26MHz to get the fvco
- The FRACTIONAL channel word (F22..F0) is
  - fractional part NF = floor( (fvco/26MHz NI)\*2^23), basically it is the mantissa of (fvco/26MHz) scaled to 23-bit

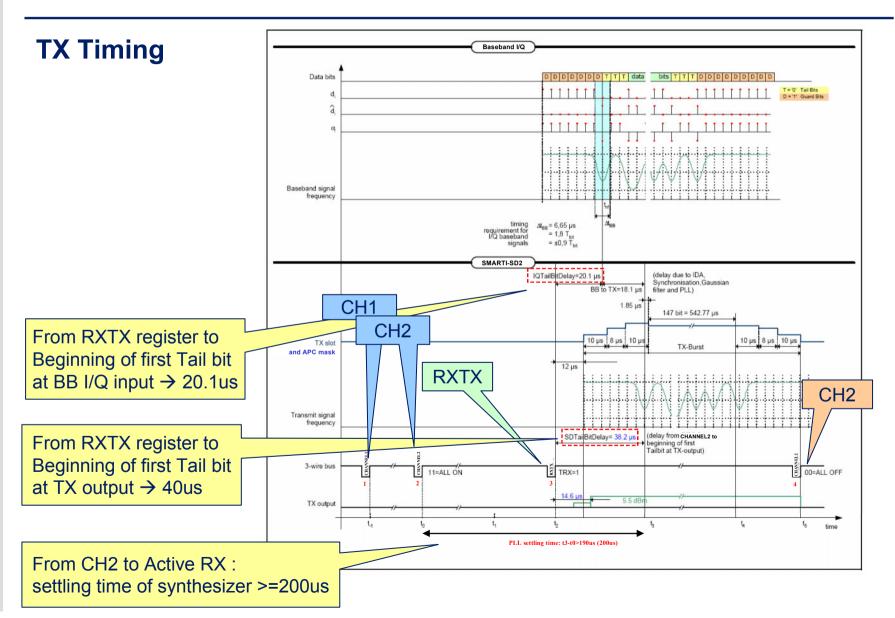
### **RX Timing**



Both CH2 and RXTX triggers EGR internal algorithms and sequencer operations must be guaranteed, >=200us

From RXTX to active RX slot, a time interval of 100us is needed to guarantee that the DC level reaches a seady state value.

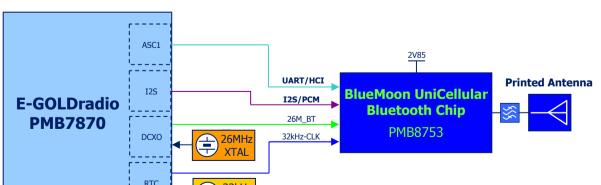
and TX modes

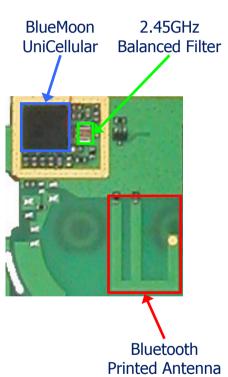


### Globe6 RF System: BlueTooth

# Infineon BlueMoon UniCellular PMB8753

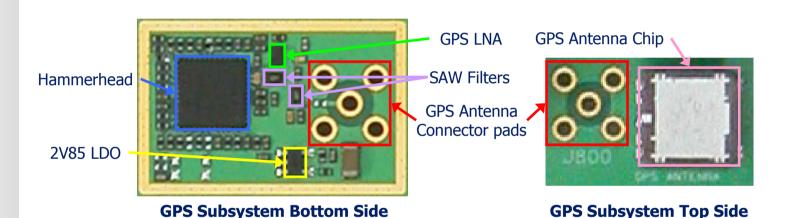
- Single chip Bluetooth 2.0 + EDR solution
- Low power design in 0.13 µm CMOS
- Integrates ARM7TDMI, RAM and patchable ROM
- On-chip voltage regulators.
- Low-IF receiver topology with integrated LNA,
   VCO and Digital demodulation

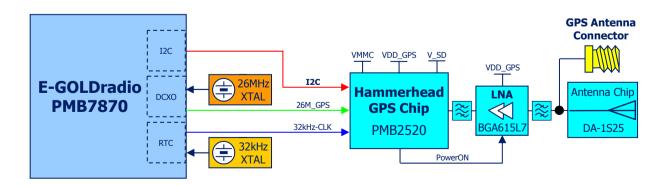




# Globe6 RF System: GPS

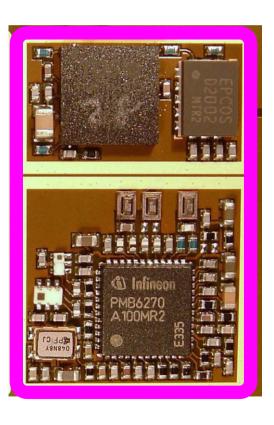
# Infineon & Global Locate's Hammerhead A-GPS PMB2520





# **Globe6 RF System: History**

BP2 Globe1 Tri-Band Transceiver



BP2 Globe2 Quad-Band Transceiver



BP2.1 Globe3
Quad-Band
Transceiver

