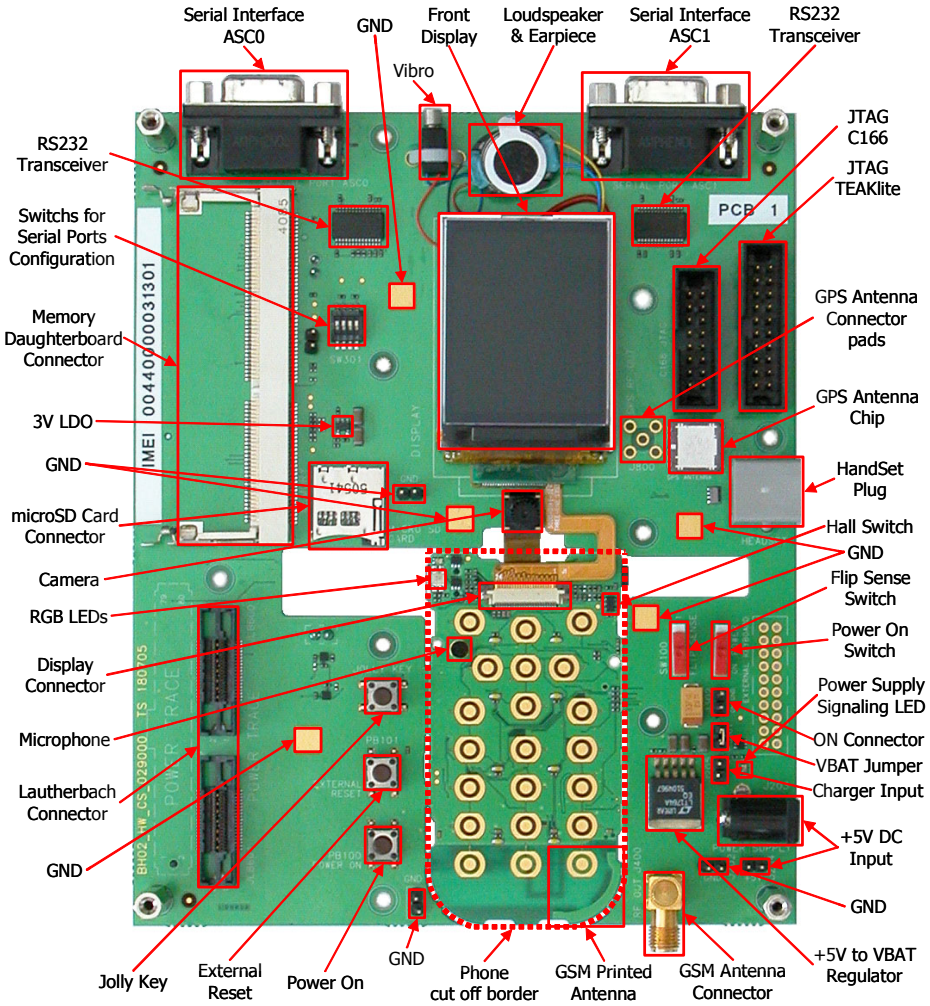
NEONSEVEN

Baseband Globe 6 presentation

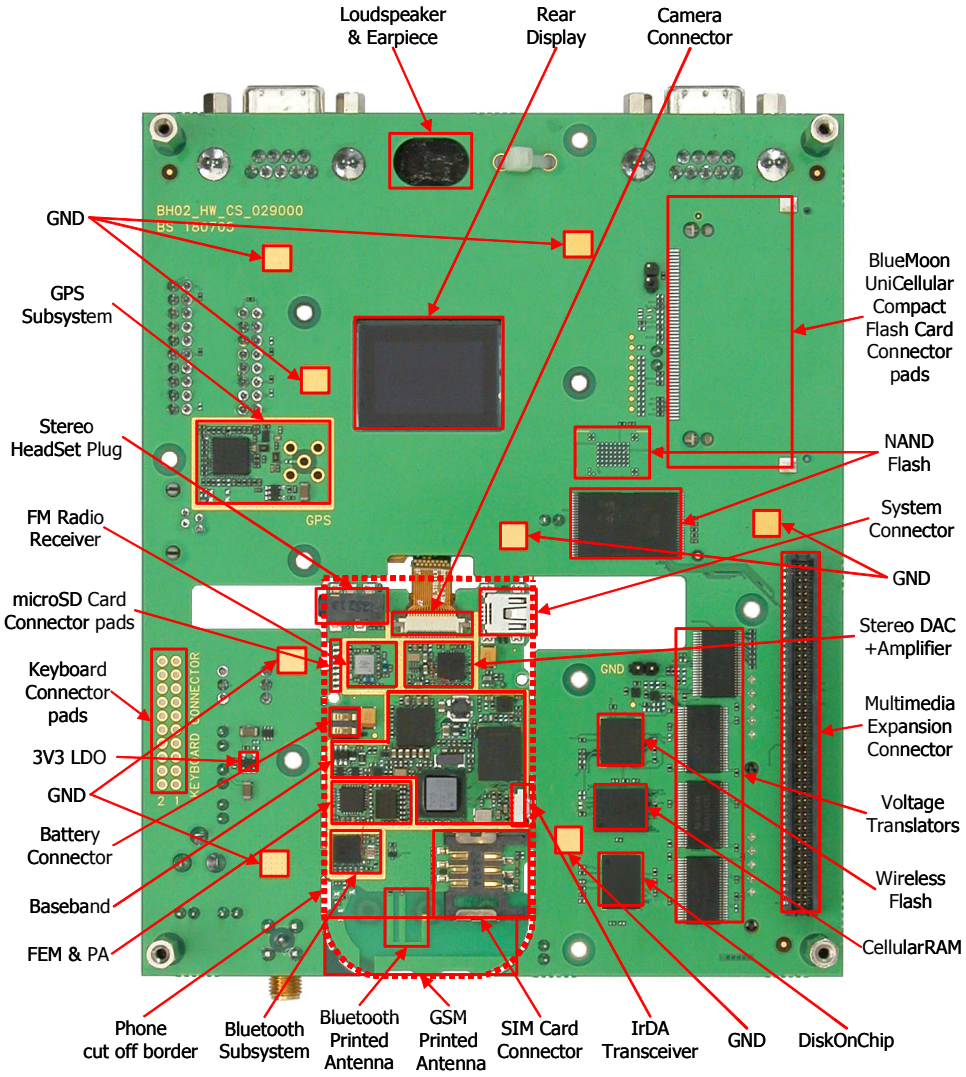
Gabriele Capello

February 2006

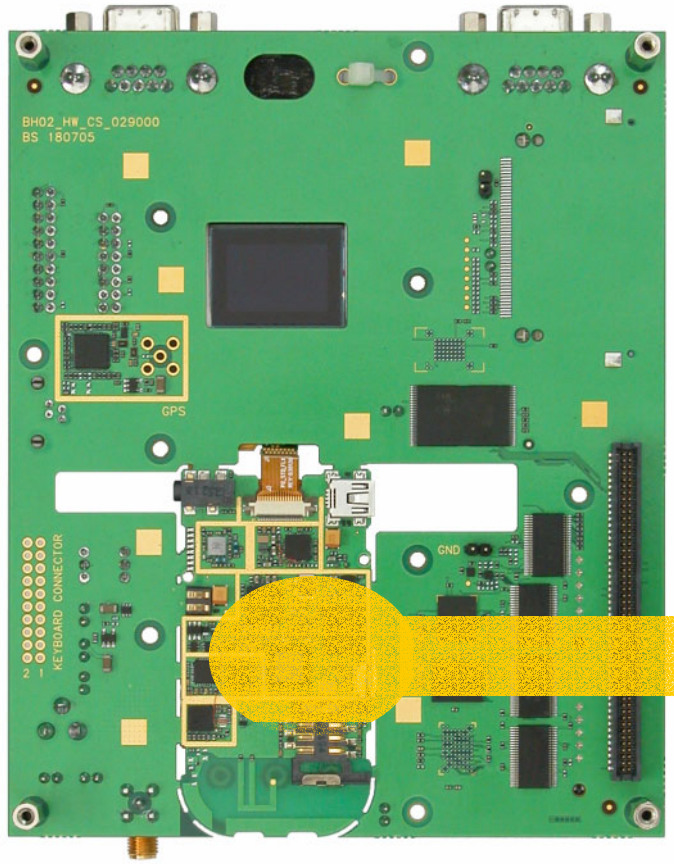
Globe 6 board front



Globe 6 board rear



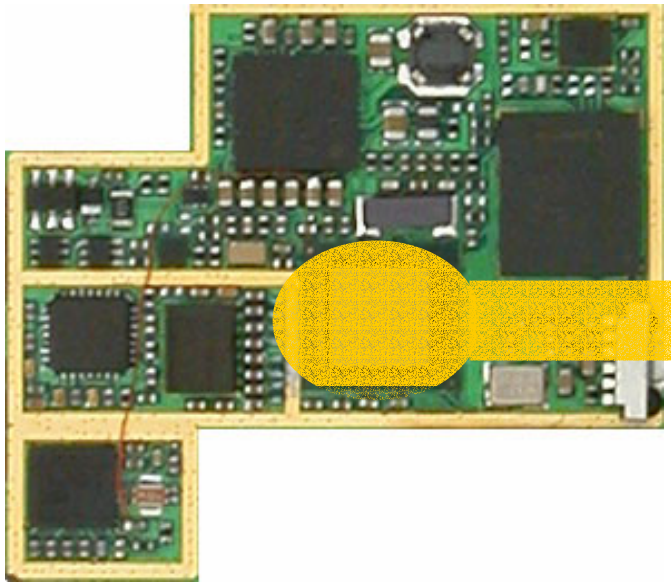
Globe 6 board rear



Baseband/RF
shielded “core”

NEONSEVEN

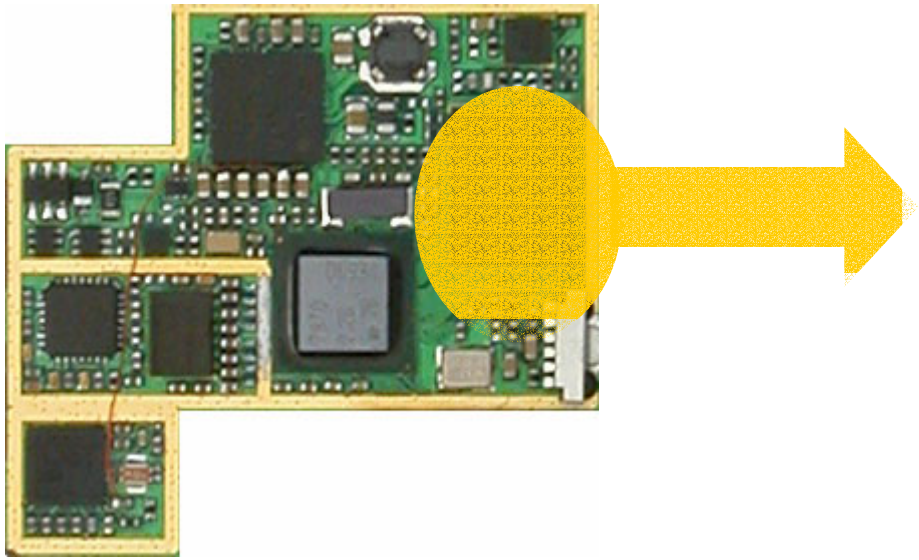
Globe 6 board rear/ Baseband shielded “core”



EGOLDRadio
PMB 7870

NEONSEVEN

Globe 6 board rear/ Baseband shielded “core”

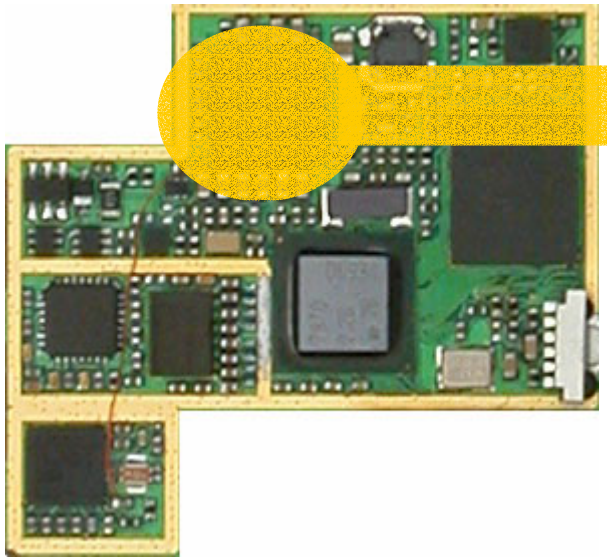


MCP “combo”

64Mbit NOR Flash
64Mbit NOR Flash
32Mbit RAM
or
128Mbit NOR Flash
32 Mbit RAM

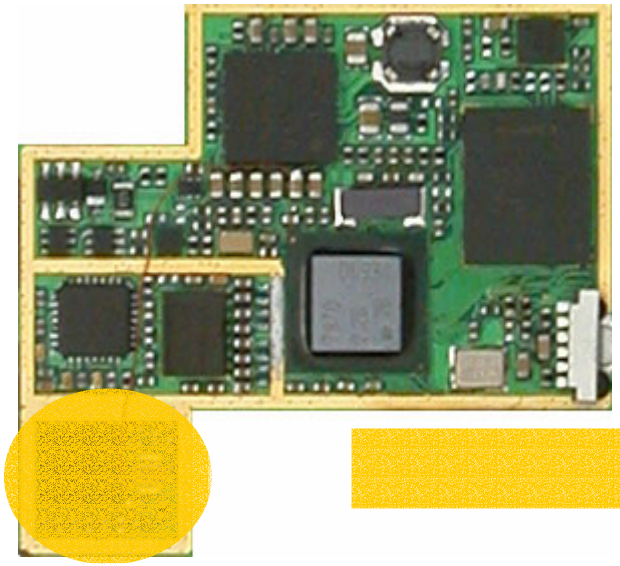
NEONSEVEN

Globe 6 board rear/ Baseband shielded “core”



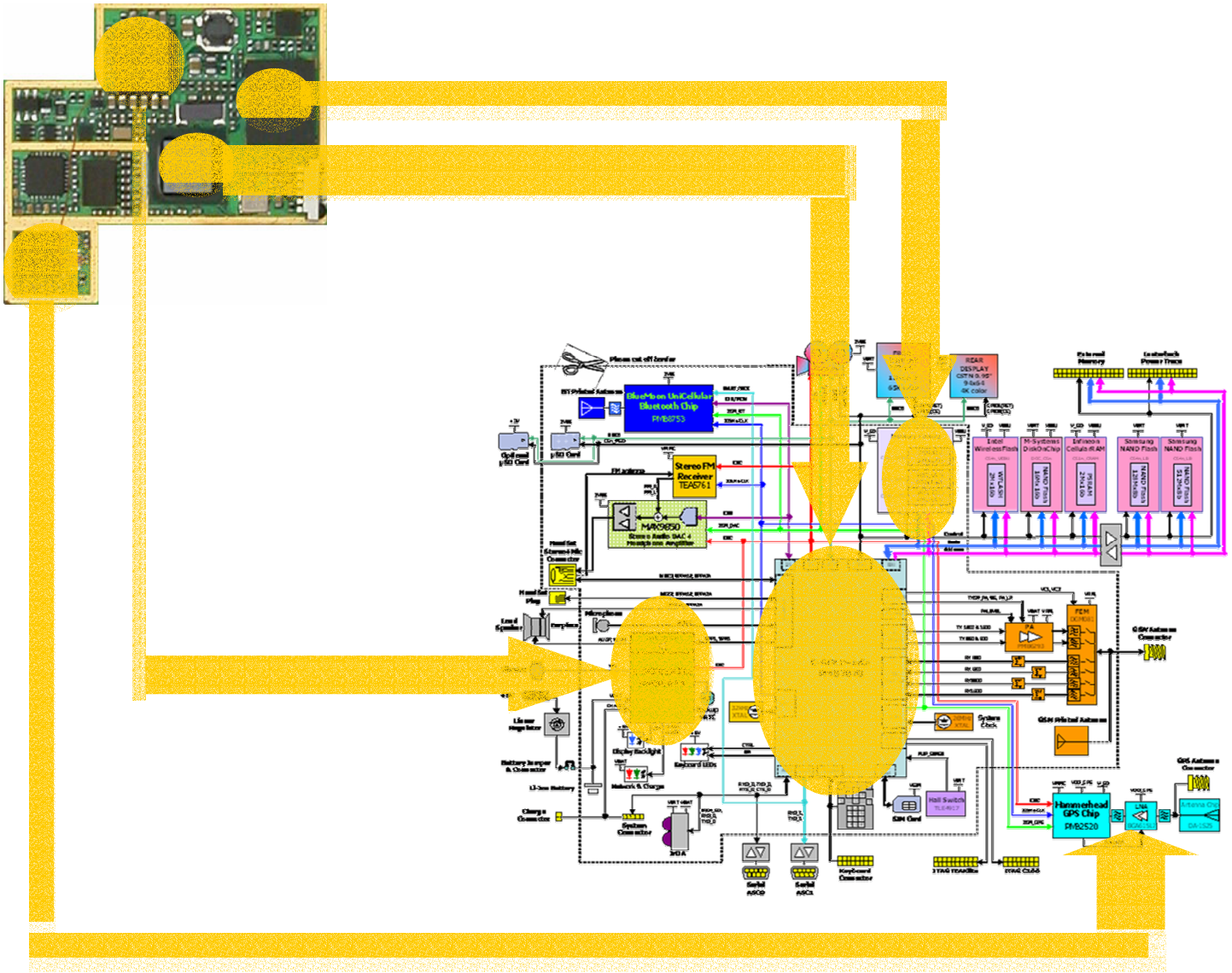
EPOWERLite
PMB6814

Globe 6 board rear/ Baseband shielded “core”



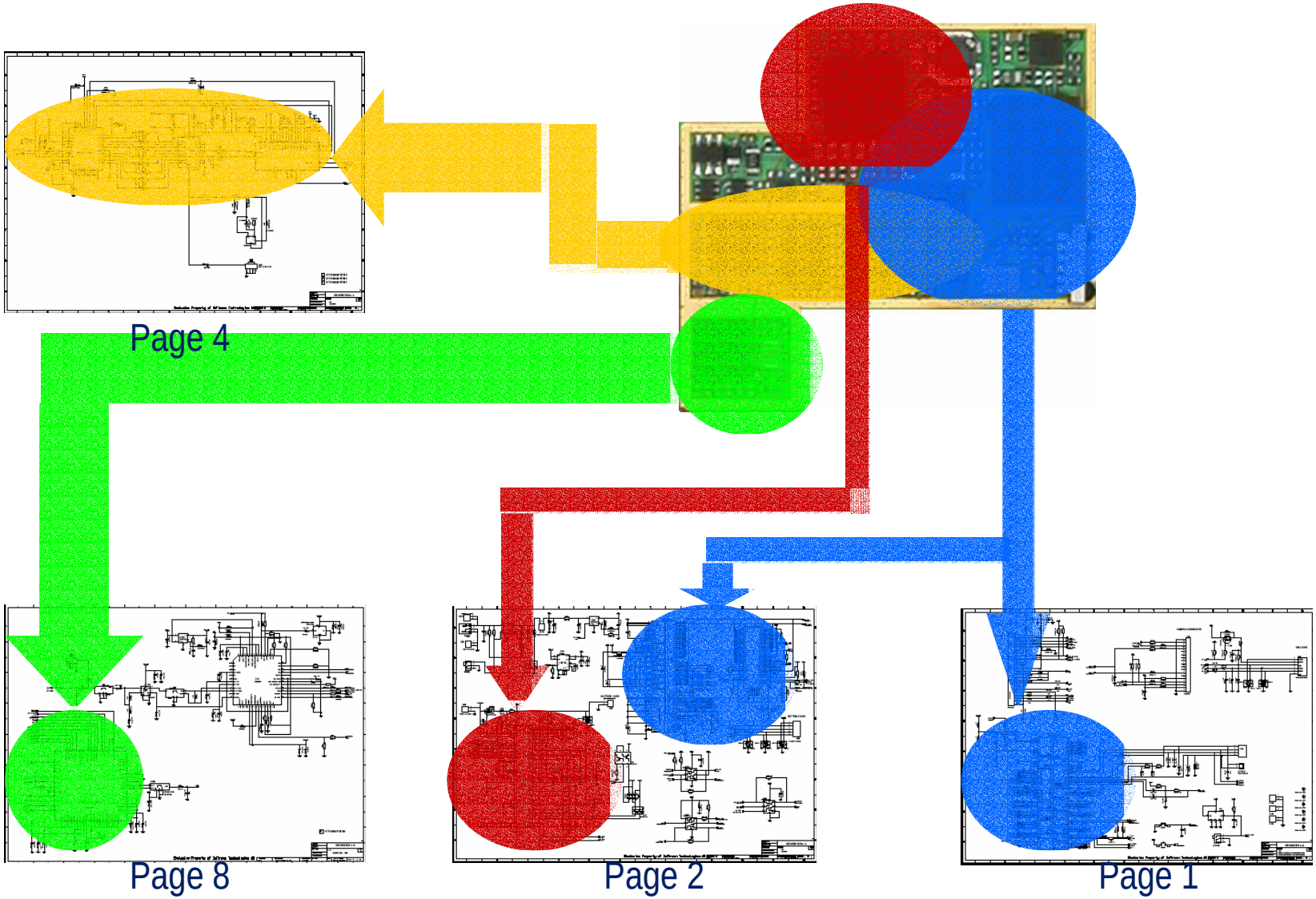
BMU
BlueMoon Universal
PMB8753

Globe 6 board rear/ Baseband shielded “core”

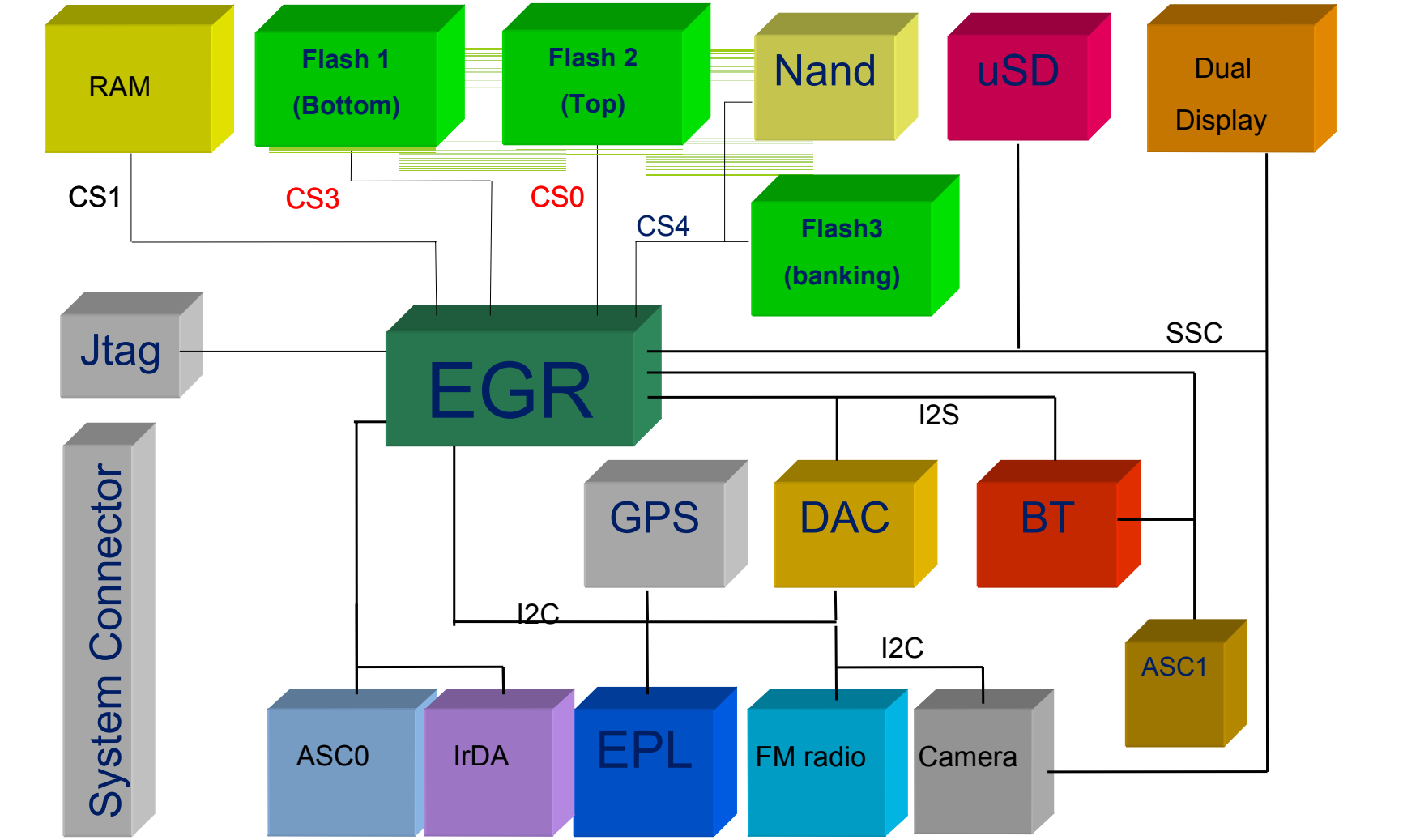


NEONSEVEN

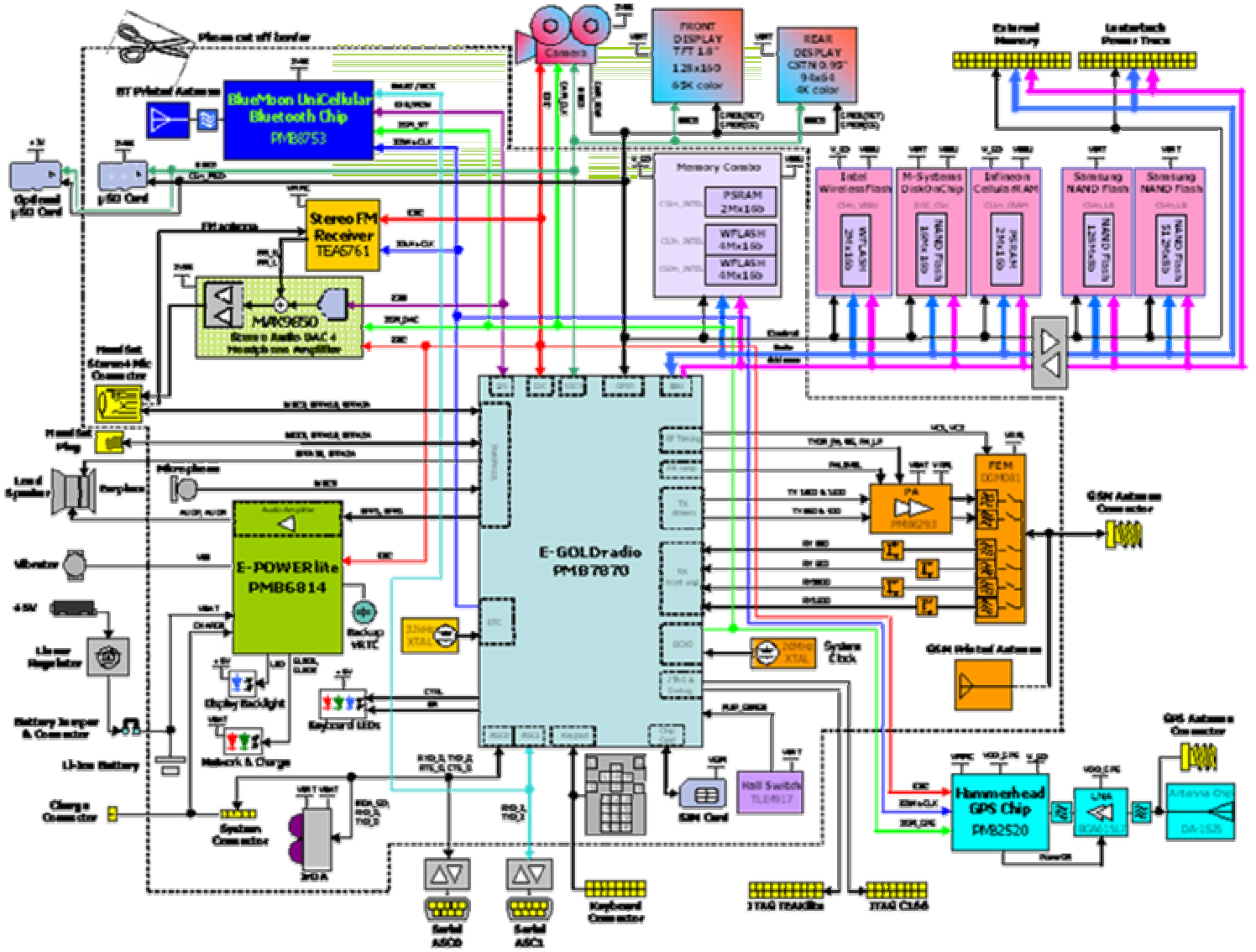
Globe 6 board rear/ Baseband shielded “core”



Globe 6 Simplified Digital Architecture
Controls point of view ("core" only)



Globe 6 Simplified Digital Architecture
Controls point of view (All)



NEONSEVEN

Globe 6 Simplified Digital Architecture

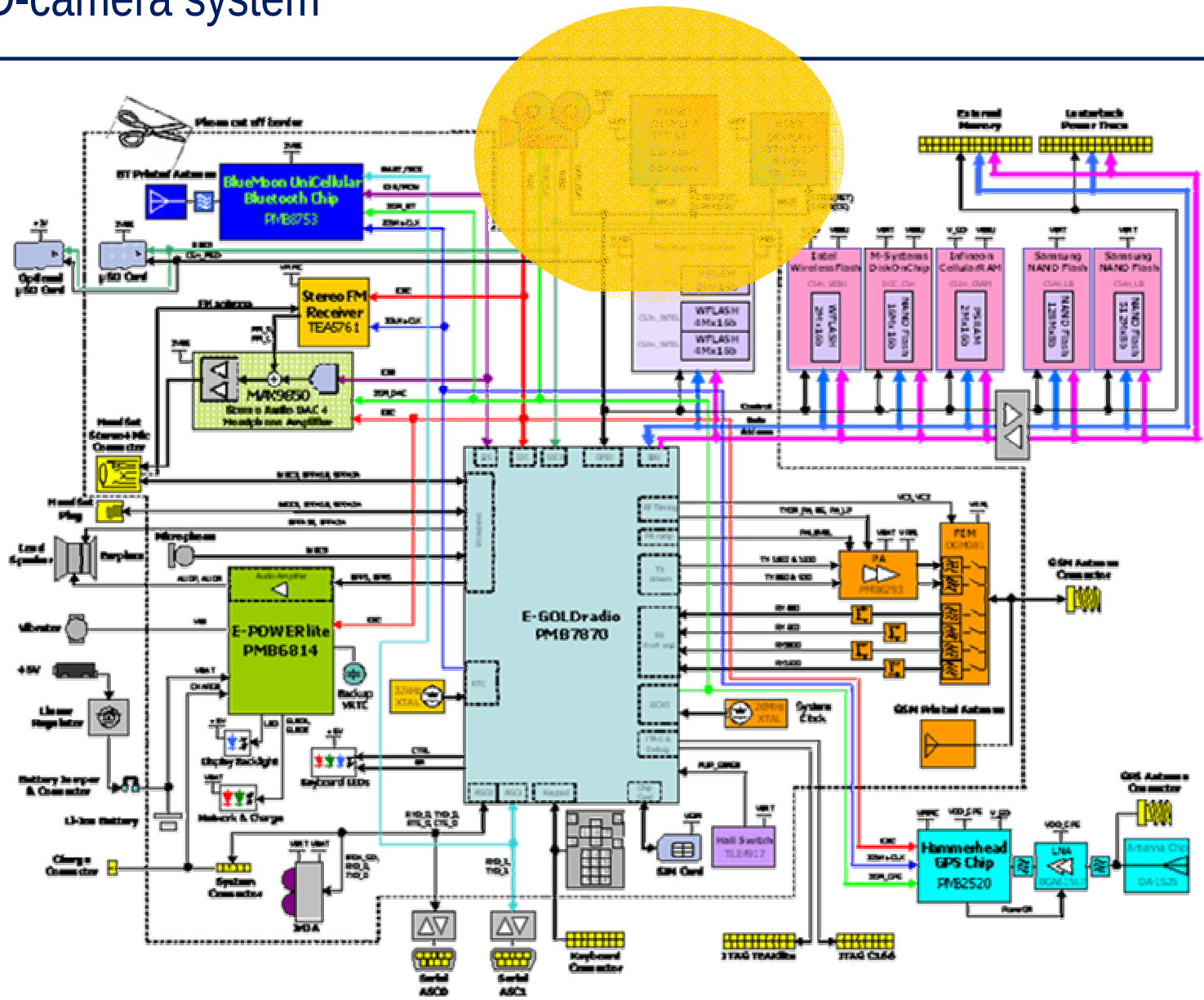
- “Core” memories can work at 1.8V/2.7V (V_SD/V_INT) selectable using a resistor. WARNING: You should mount the correct type of memory on board.
- External memories bus should use the same voltage of “core” memories
- Peripherals works at 2.7V

NEONSEVEN

Globe 6 Simplified Digital Architecture

- Basic rules used for peripherals interfacing:
  - use the lowest cost solution if possible → use only passive components for interfacing
  - try to use less component as possible (less component means more board mounting reliability)

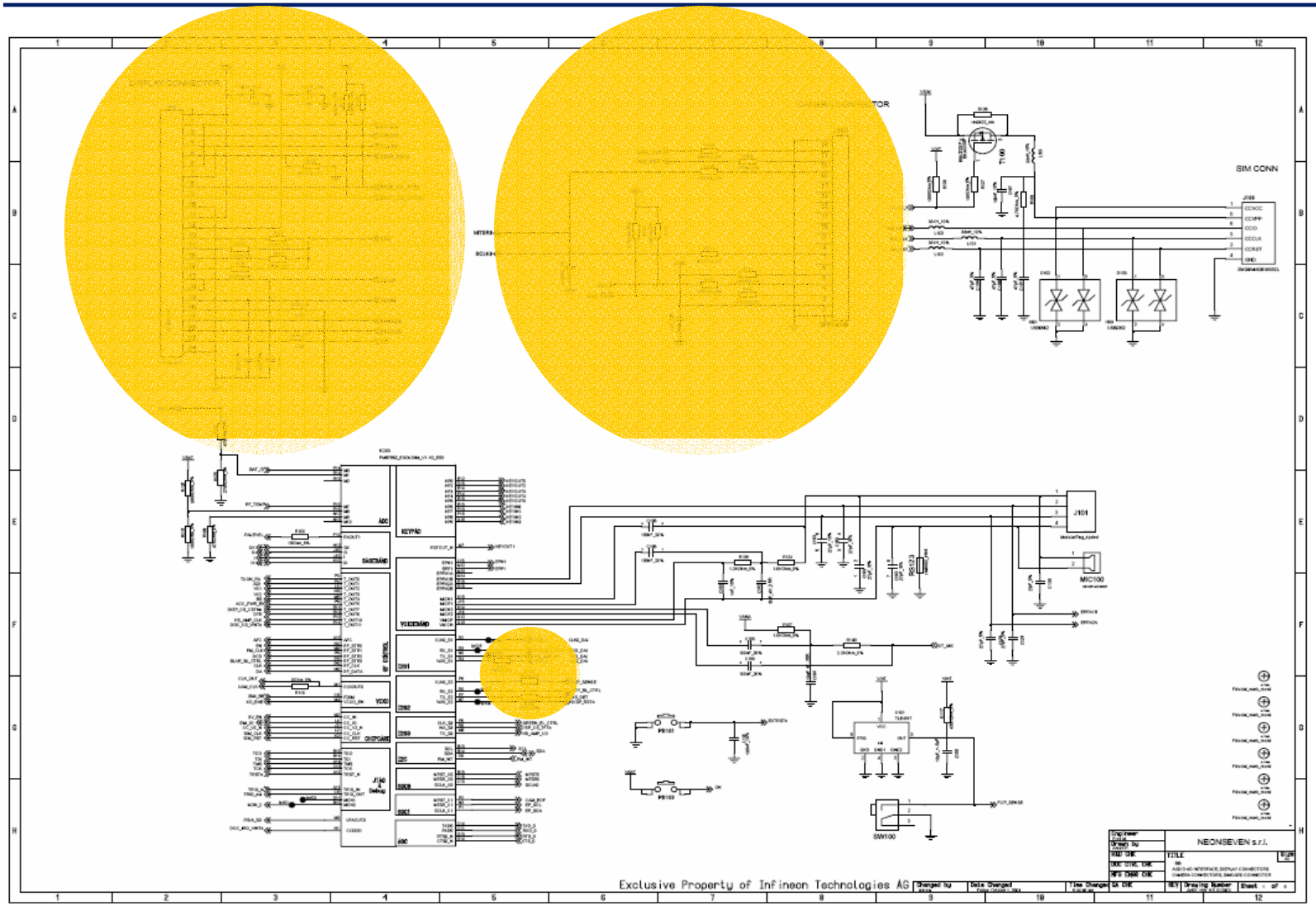
Globe 6 Simplified Digital Architecture
LCD-camera system



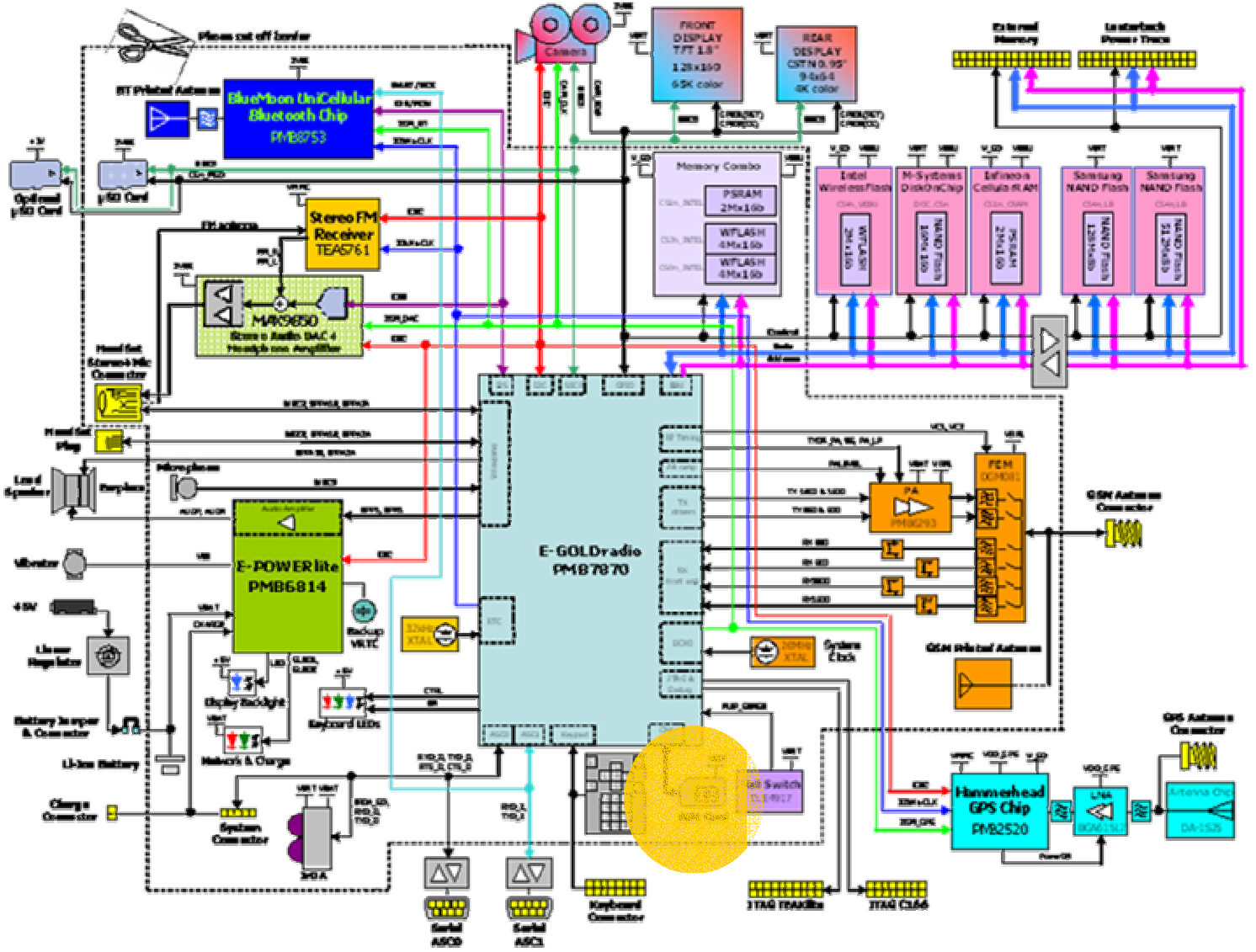
Globe 6 Simplified Digital Architecture
LCD-camera system

- SSC used as common bus between Camera, Main and secondary display
- I2C used to control camera
- Scenarios ("→" data direction on SSC bus)
  - Image transfer on main display: EGR→Main display
  - Image transfer on secondary display: EGR→Secondary display
  - Camera Preview: Camera→Main display
  - Photo acquisition: Main display→EGR

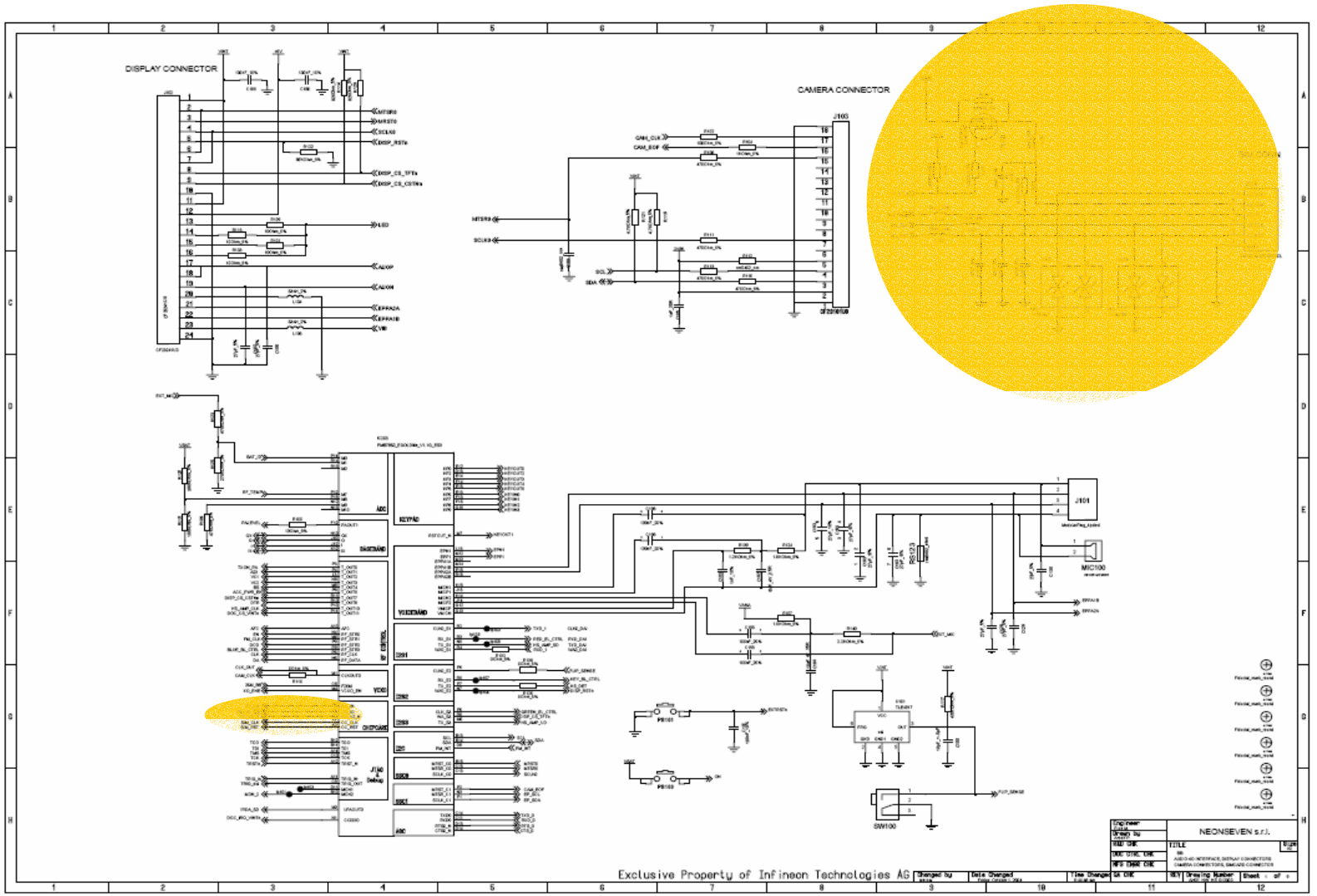
Globe 6 Simplified Digital Architecture
LCD-camera system



Globe 6 Simplified Digital Architecture
SIM system

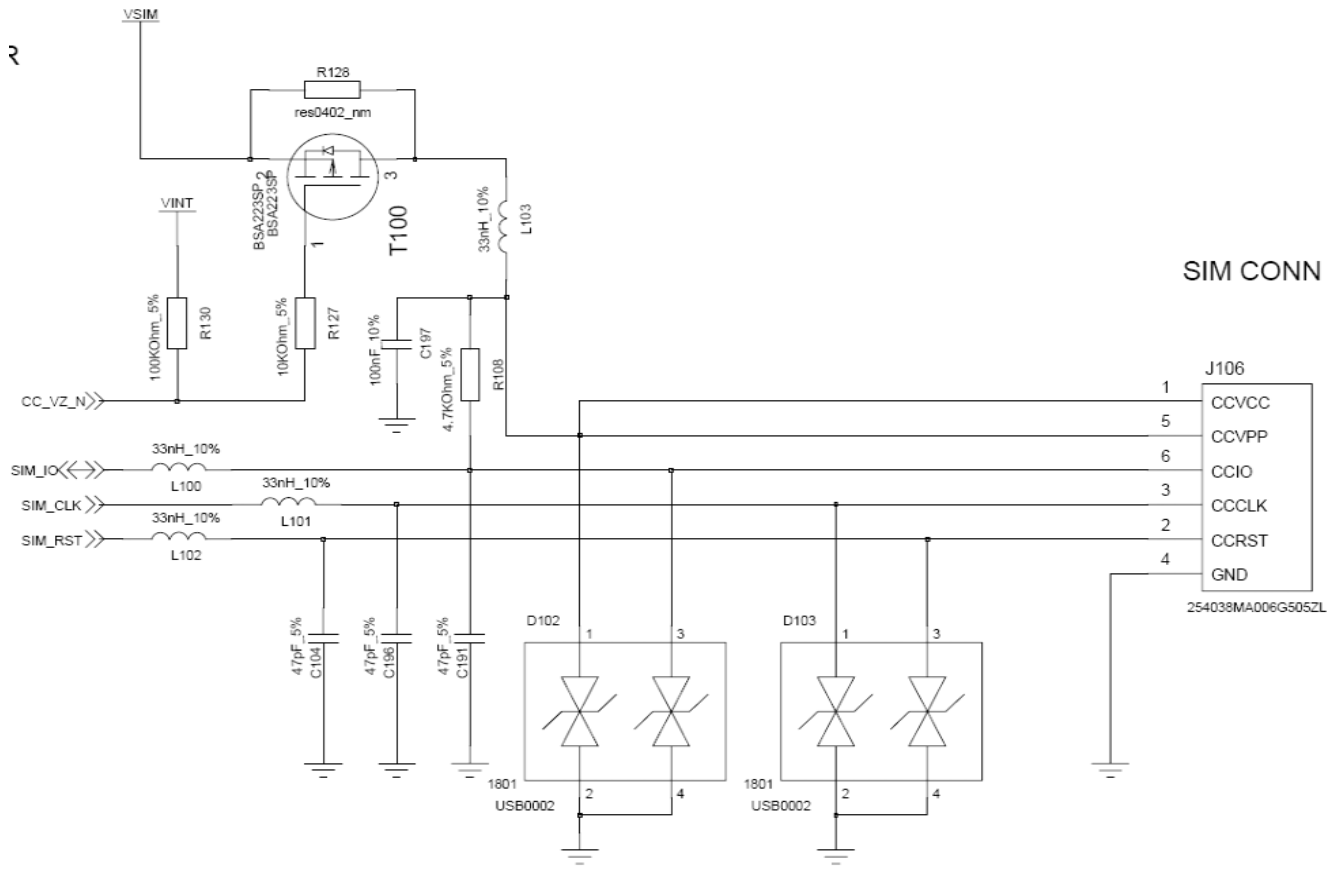


Globe 6 Simplified Digital Architecture
SIM system

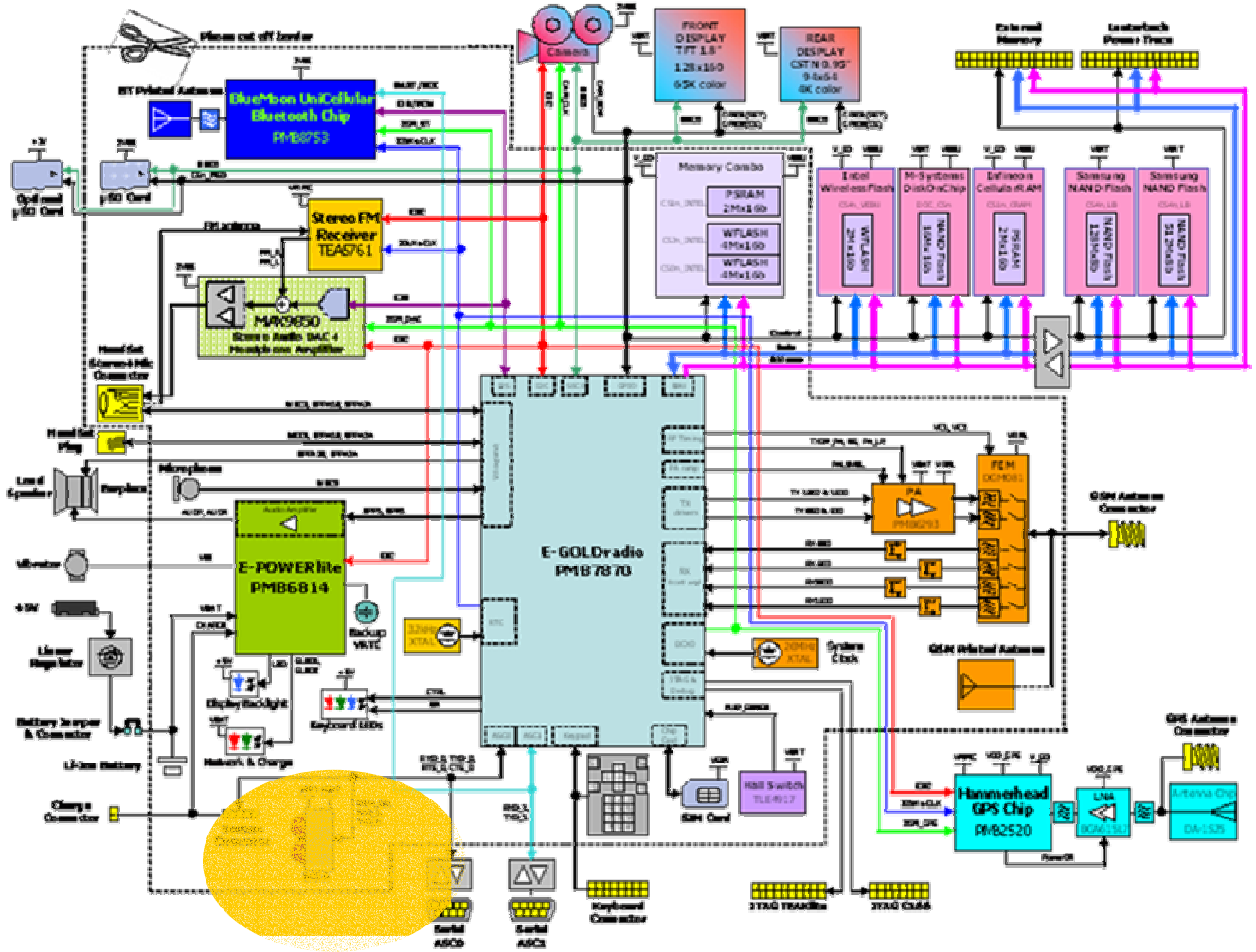


Globe 6 Simplified Digital Architecture
SIM system

- Quite a standard connection except for a PMOS that isolate Sim power supply from VSIM



Globe 6 Simplified Digital Architecture
IRDA system

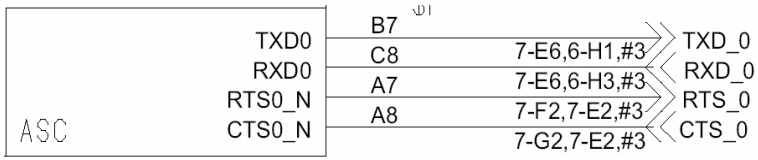


Globe 6 Simplified Digital Architecture
IRDA system

- EGR IRDA is mapped on ASC0 interface → IRDA and data communication should work exclusively each other
- EGR boot the FW from ASC0 so the board should:
  - Enable boot from data cable and disable IRDA transceiver
  - After boot, EGR should be able to enable/disable IRDA transceiver (EGR GPIO has been used to enable/disable different interfaces)

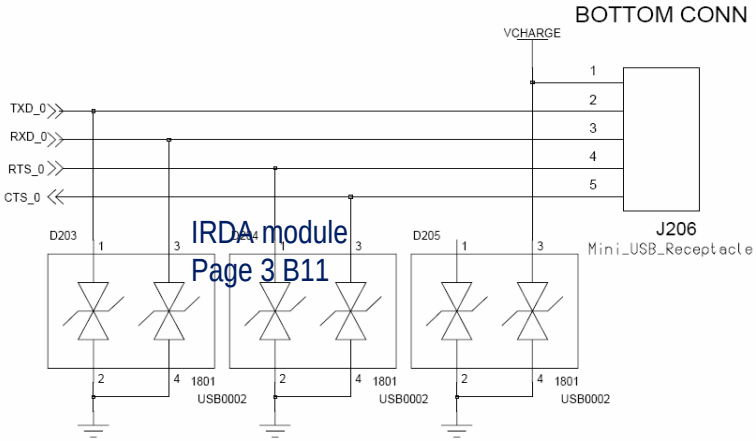
Globe 6 Simplified Digital Architecture
IRDA system

ASC 0 on EGR
Page 1 H4



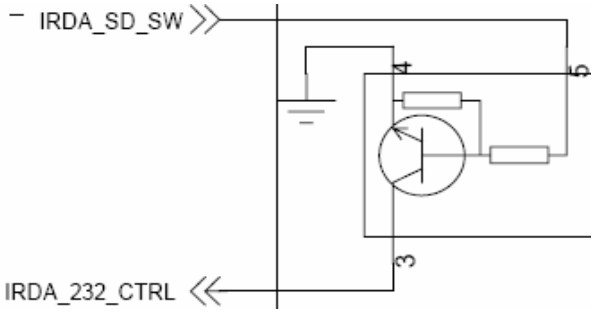
IRDA_SD
control signal
Page 8 D2,
now is
genereated by
BT chip

Bottom Connector
Page 2 E11

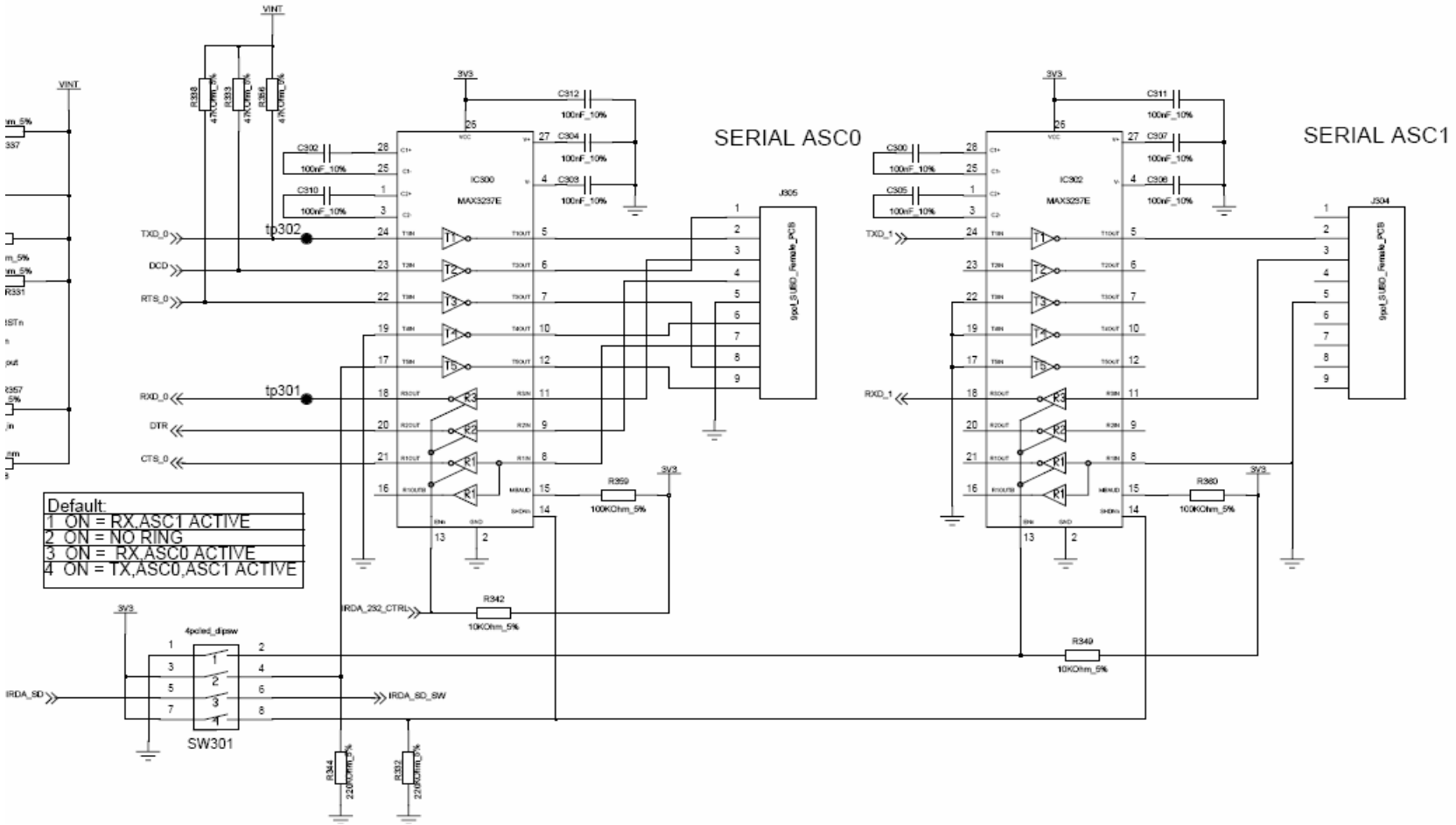


IRDA module
Page 3 B11

T203 IRDA_SD_SW
inverter
Page 3 D11



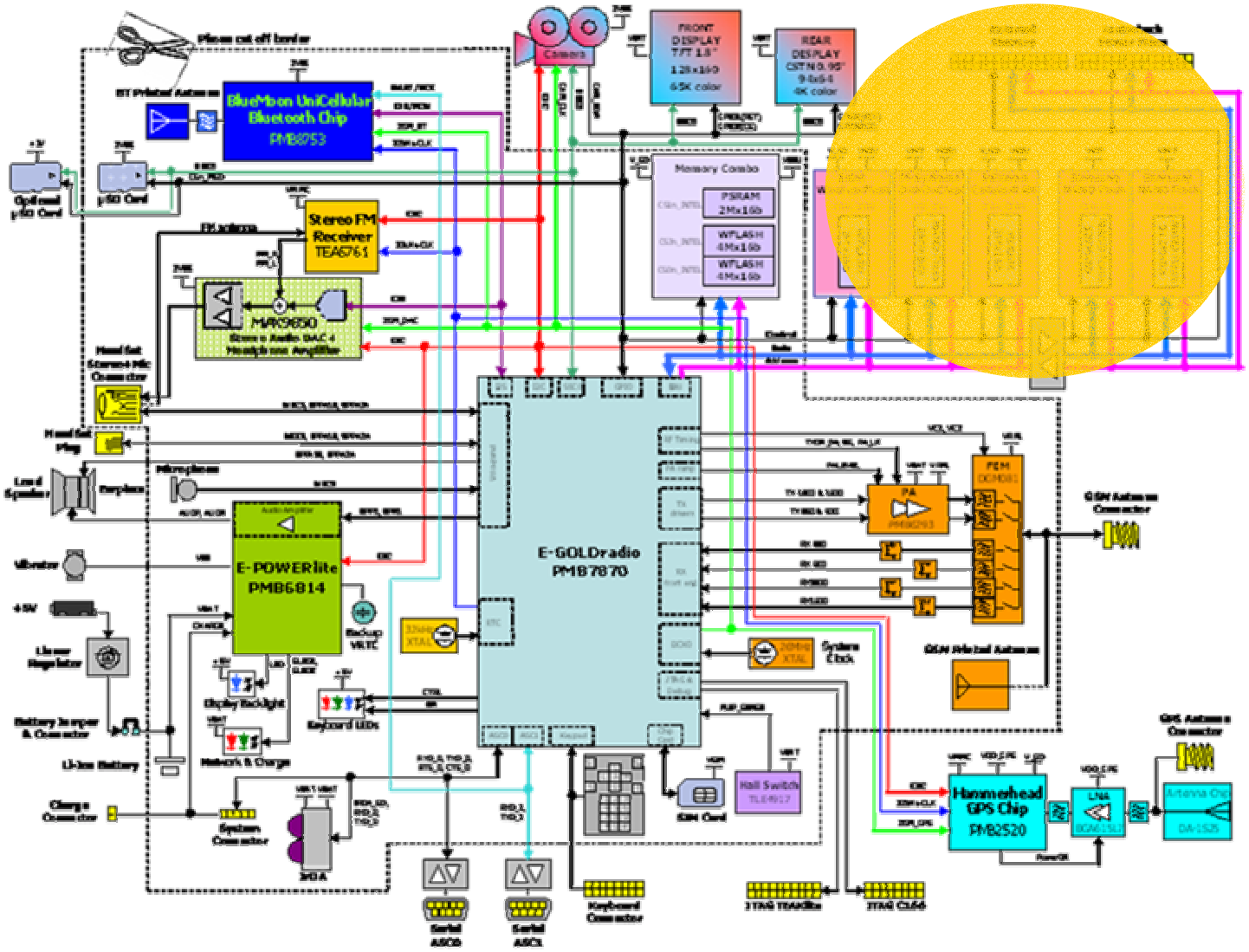
Globe 6 Simplified Digital Architecture
IRDA system



Globe 6 Simplified Digital Architecture
ASC 0/1

- MAX3237E has been used to translate ASC 2.7V signals to RS232 voltages up to 1Mbaud
- ASC1 port mapped as alternative function of I2S1
- DAI tests could be on I2S1 or I2S2 depending of a FW patch, in any case is possible to isolate colliding signals

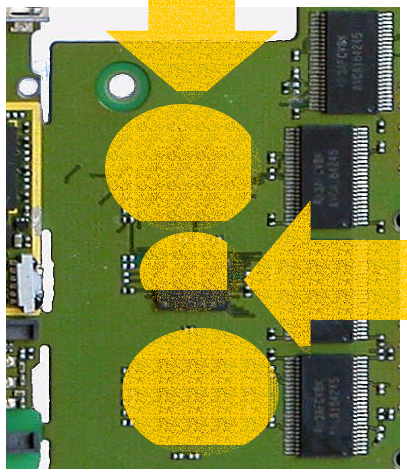
Globe 6 Simplified Digital Architecture
Alternate Memory System (some common memories)



Globe 6 Simplified Digital Architecture
Alternate Memory System (some common memories)

32MBit NOR

PH28F320W18TD60



cRAM 32MBit:

HYE18P32160AC

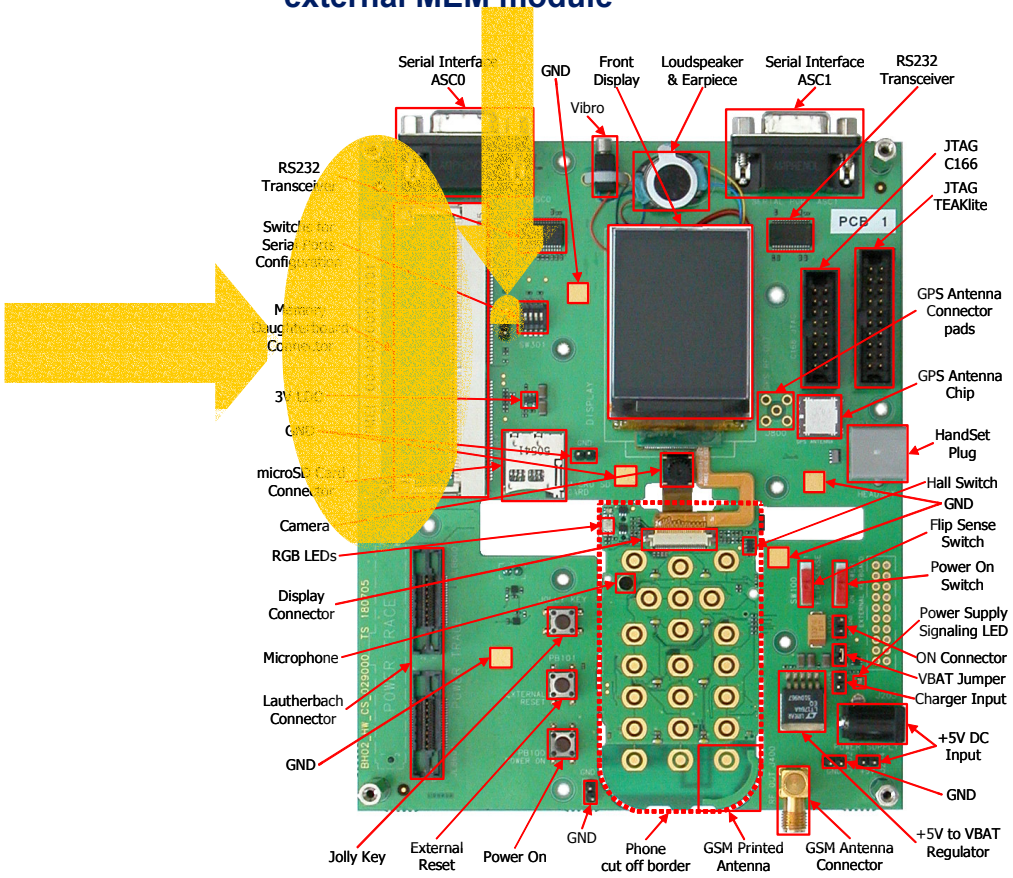
DiskOnChip:

MD5832-d256-V3Q18-X-P

Globe 6 Simplified Digital Architecture
Alternate Memory System (some common memories)

Infineon Memory connector

Put a jumper to enable writing to external MEM module



Globe 6 Simplified Digital Architecture
Some possible memory combinations

	CS0	CS1	CS3	CS4	Notes
Intel Combo	Intel Combo 64MBit W NOR	Intel Combo 32MBit cRAM	Intel Combo 64MBit W NOR	DoC/uSD chip select/Nand/Banking Flash/External board External Board Mem	
Infineon Combo	Infineon 128MBit NOR	Infineon 32MBit cRAM		DoC/uSD chip select/Nand/Banking Flash/External board External Board Mem	Resolder over Intel Combo
Internal NOR + external cRAM	Intel Combo 64MBit W NOR	Infineon 32MBit cRAM	Intel Combo 64MBit W NOR	DoC/uSD chip select/Nand/Banking Flash/External board External Board Mem	
External NOR + external cRAM	Intel 32MBit W NOR	Infineon 32MBit cRAM		DoC/uSD chip select/Nand/Banking Flash/External board External Board Mem	
Infineon Memory on Memory connector	External Board Mem	External Board Mem	External Board Mem	DoC/uSD chip select/Nand/Banking Flash/External board External Board Mem	

NEONSEVEN

- Questions ?

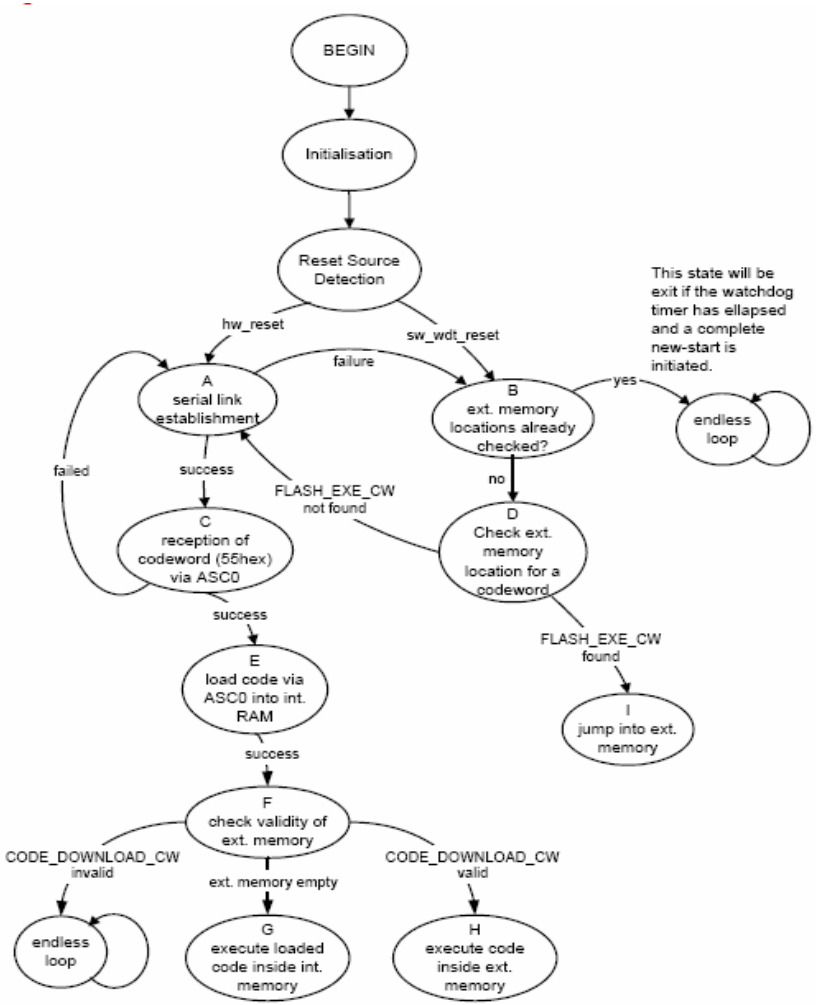
NEONSEVEN

Baseband Training part 2

Gabriele Capello

February 2006

EGR Boot up sequence



EGR Boot up sequence

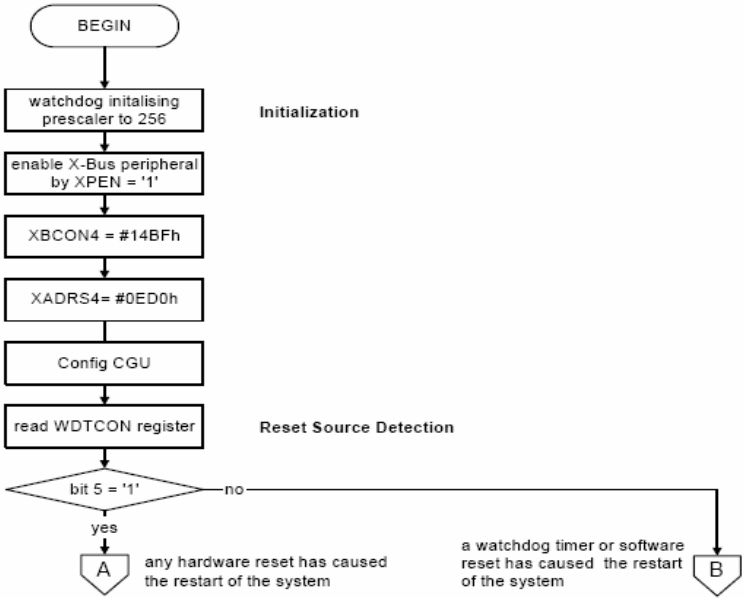
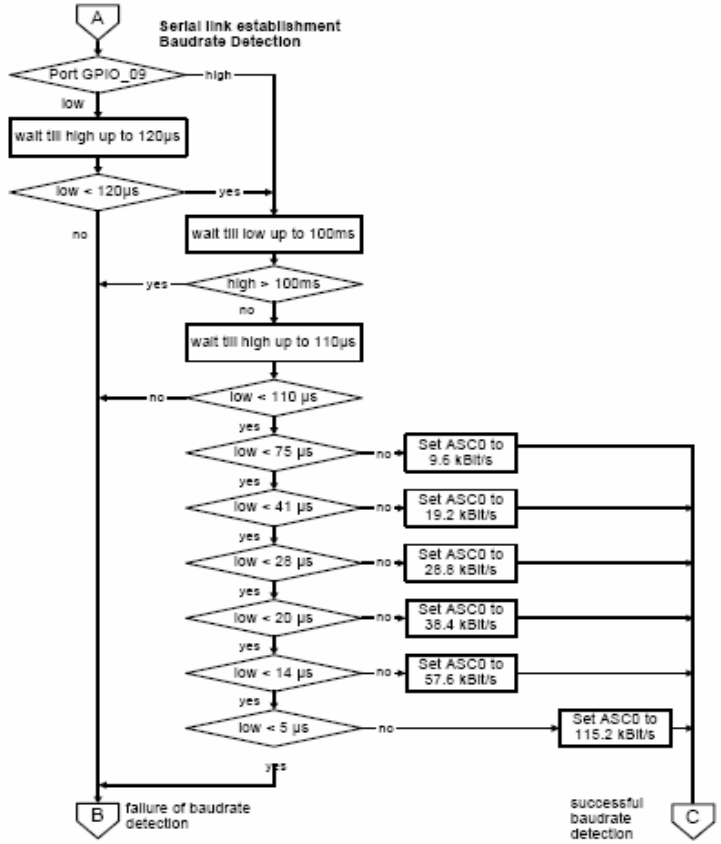


Figure 16-3 Serial Link Establishment



EGR Boot up sequence

Figure 16-4 Reception of Codeword via ASC0

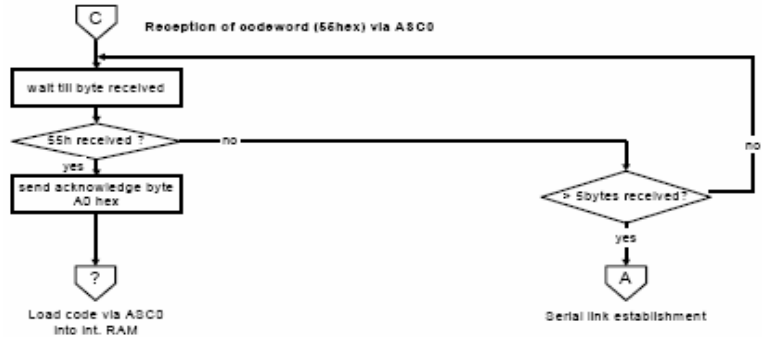
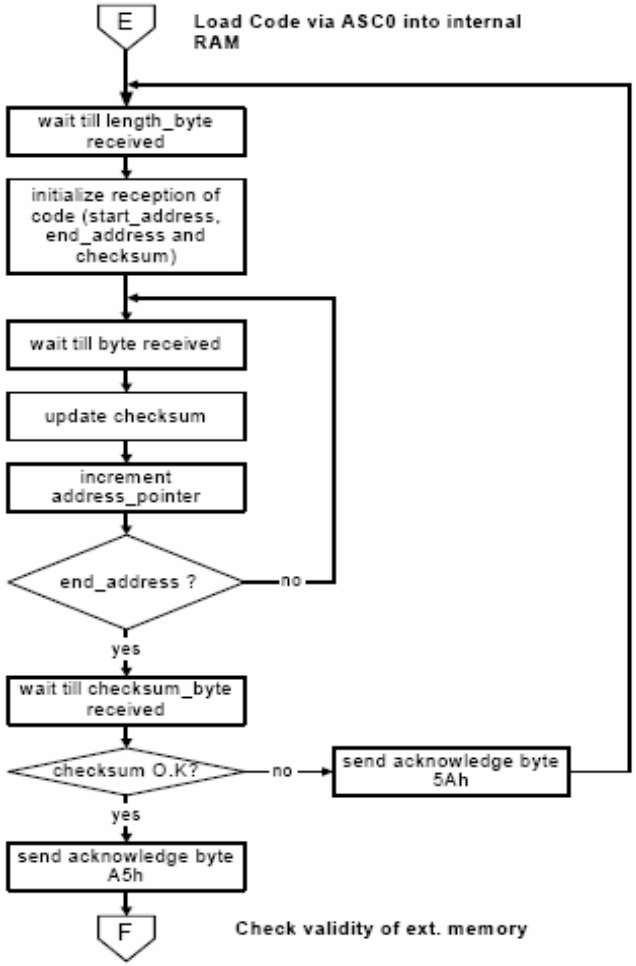
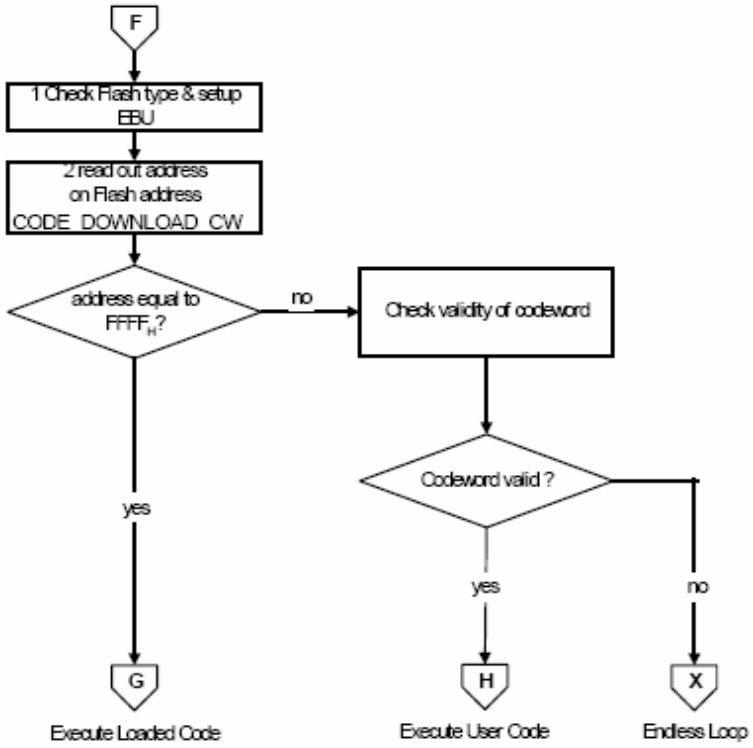
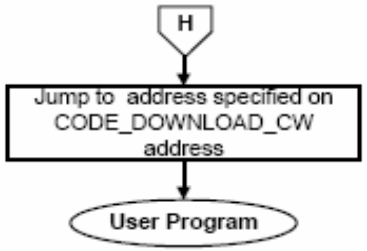


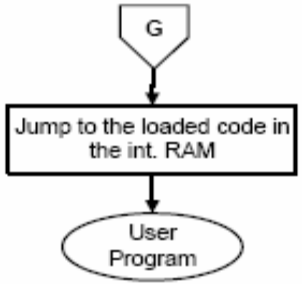
Figure 16-6 Load Code via ASC0 into Internal RAM



EGR Boot up sequence

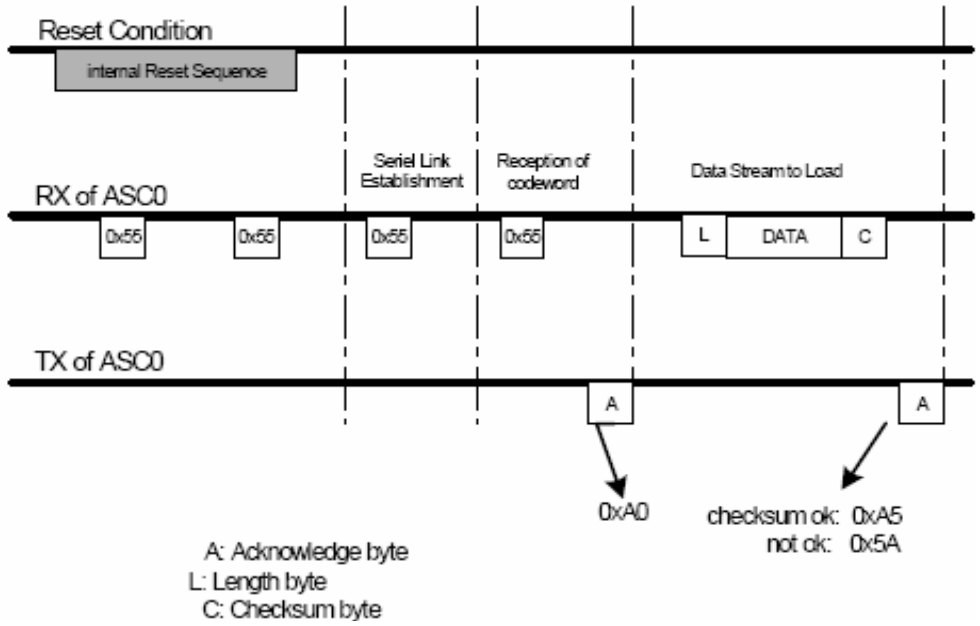






EGR Boot up sequence

Figure 16-10 Boot Sequence



EGR Boot up sequence

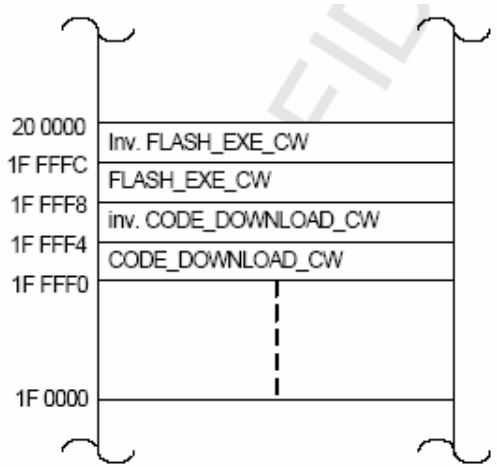


Table 16-1 Internal Boot Options

Flash Type	TRIG_IN (MCD_BBS.TRIG_IN_LATCH)	MON1 (MODR.bit0)	EBU Configuration
8-bit non-muxed NOR	0	1	BUSCON0 = 0400_H
16-bit non-muxed NOR	0	0	BUSCON0 = 0480_H
8-bit NAND	1	1	BUSCON1 = 0400_H ADDRSEL1 = 8000_H
16 bit NAND	1	0	BUSCON1 = 0480_H ADDRSEL1 = 8000_H

Figure 16-15 Codeword Address

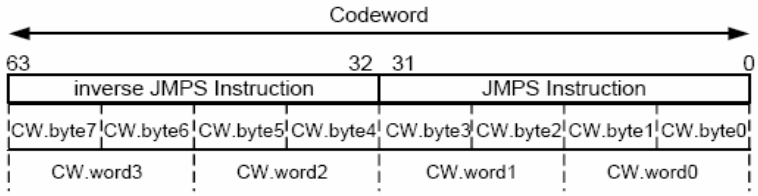
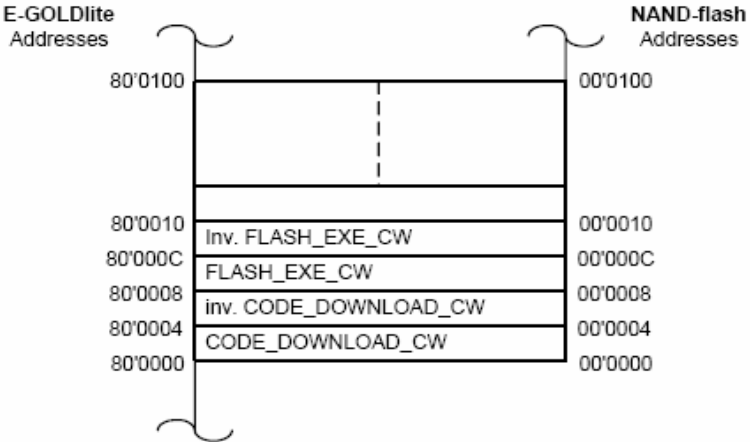
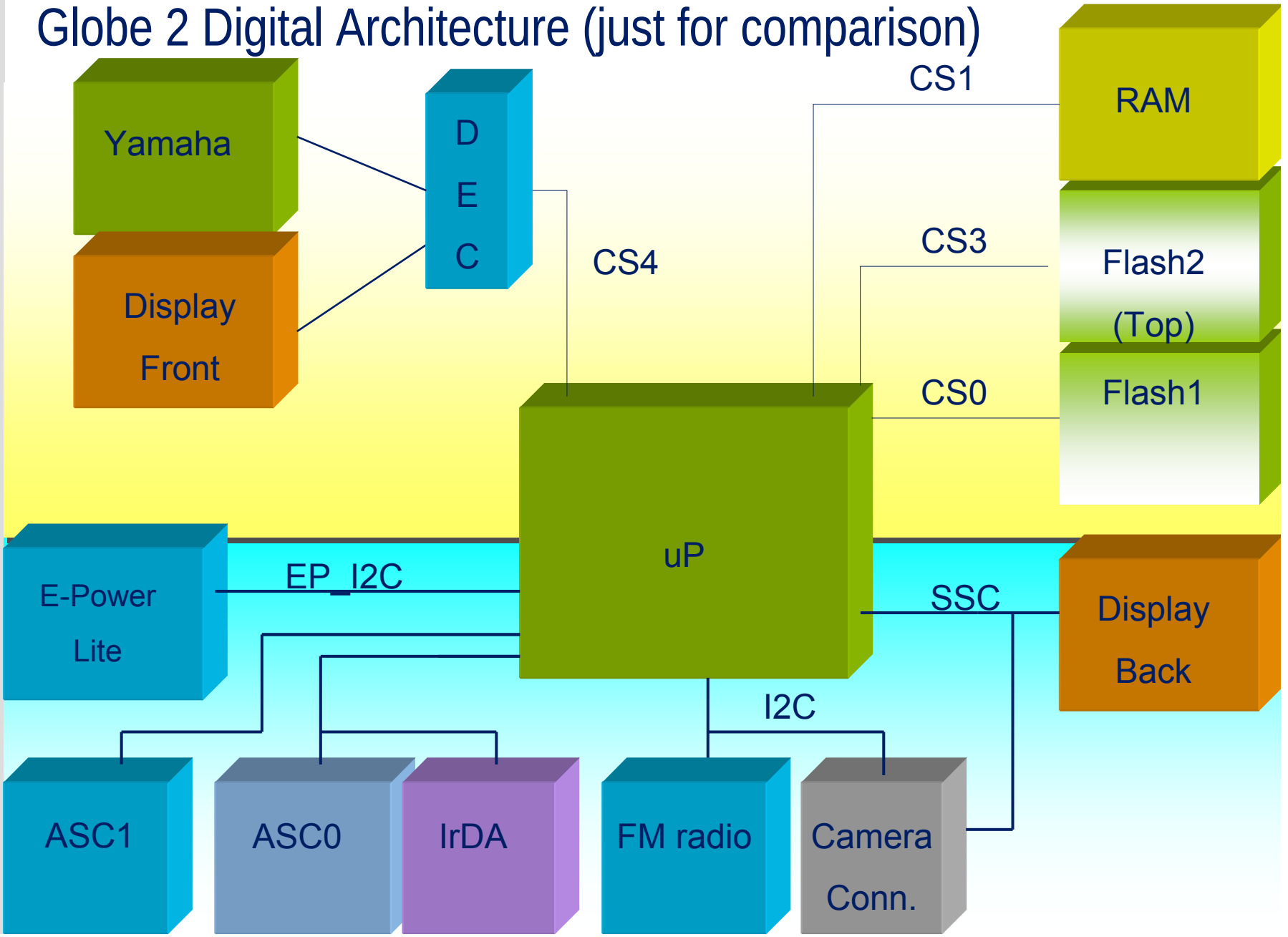


Figure 16-13 Memory Map of NAND Flash Memory



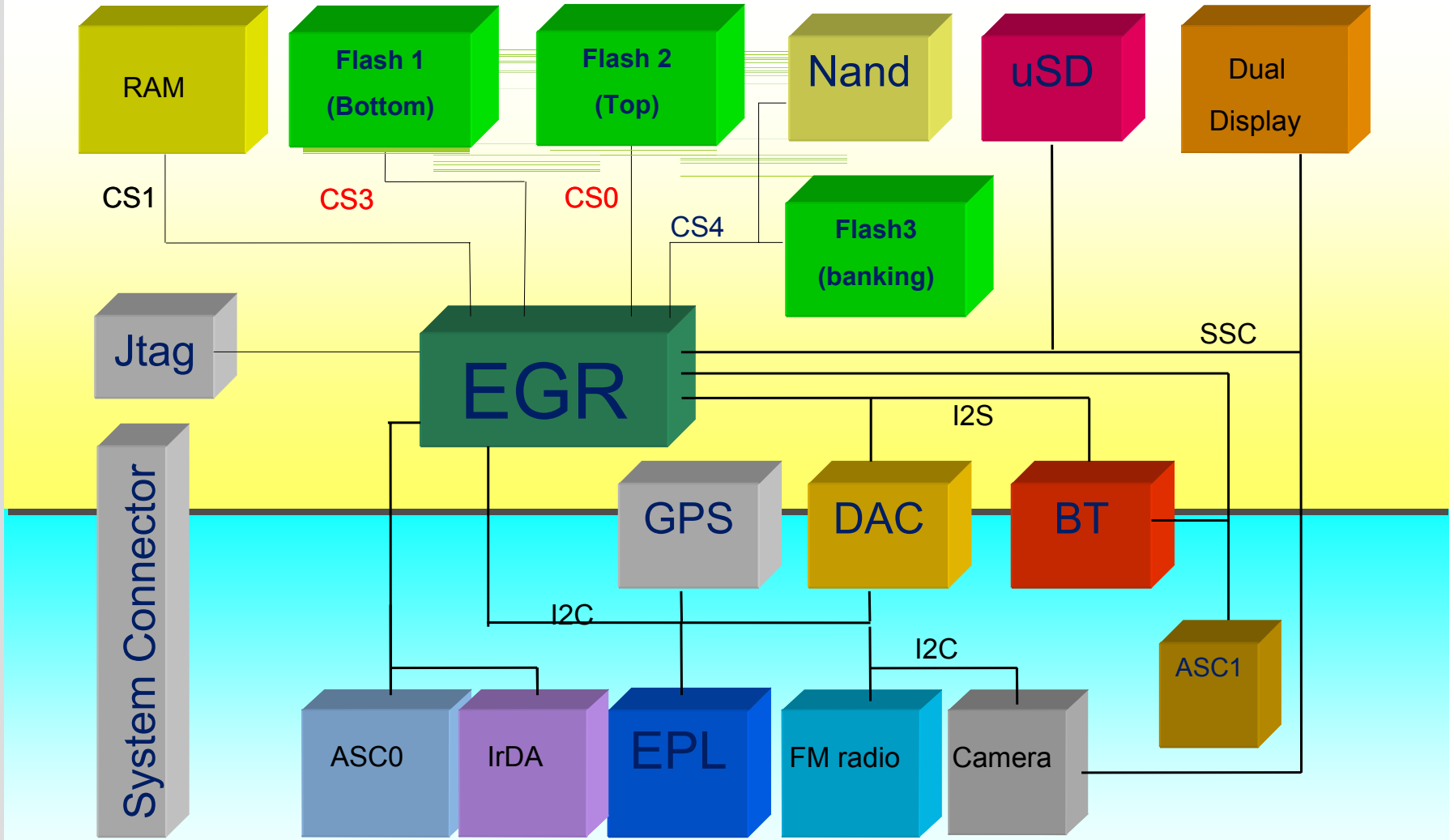
NEONSEVEN

Globe 2 Digital Architecture (just for comparison)

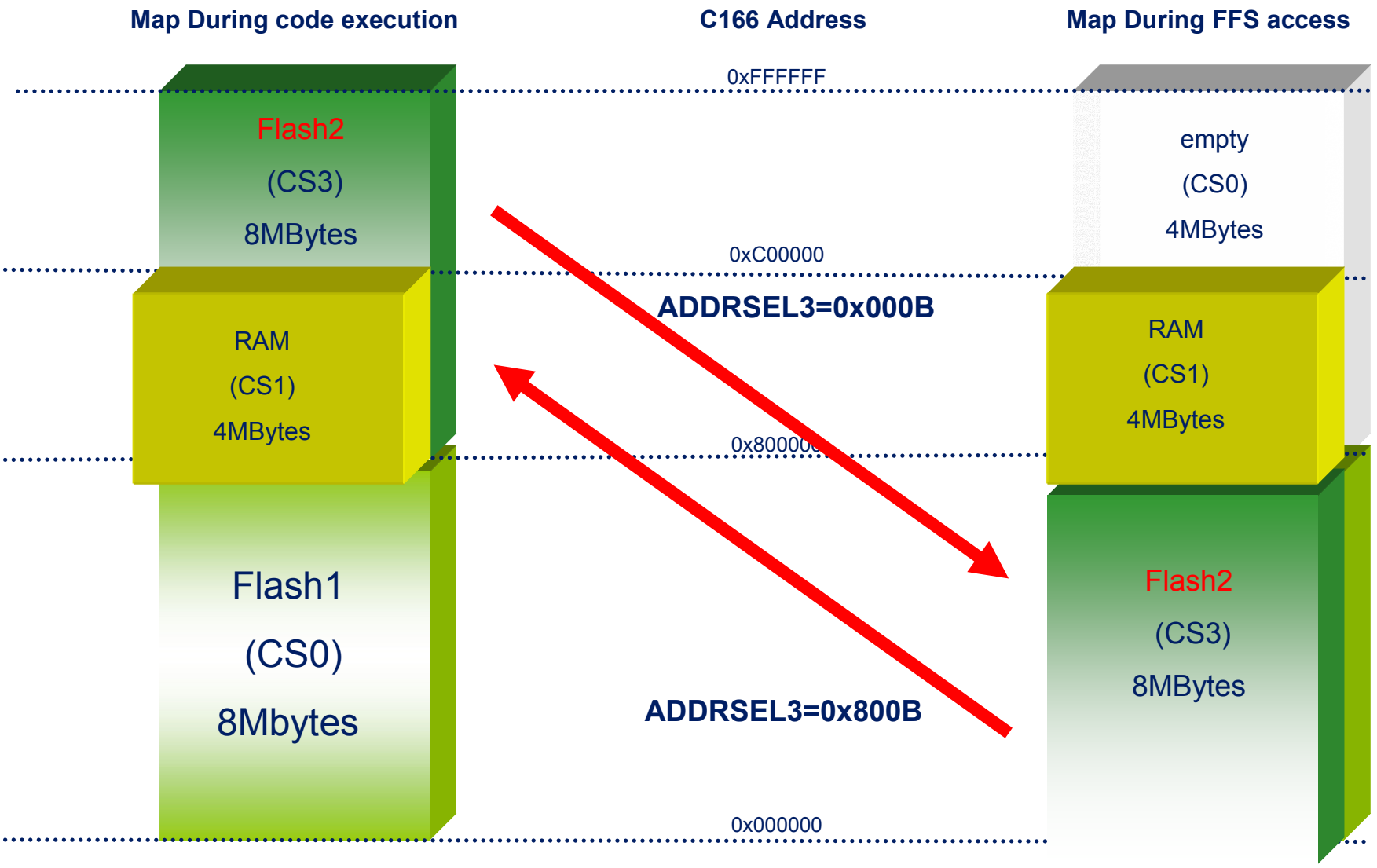


NEONSEVEN

Globe 6 Digital Architecture



GLOBE6 Sys Resources and Memory map
DWD Flash Banking (same as on GLOBE2)



GLOBE3 Sys Resources and Memory map
CS4n: GLOBE2(front display,Yamaha) →GLOBE3 (DiskOnChip)

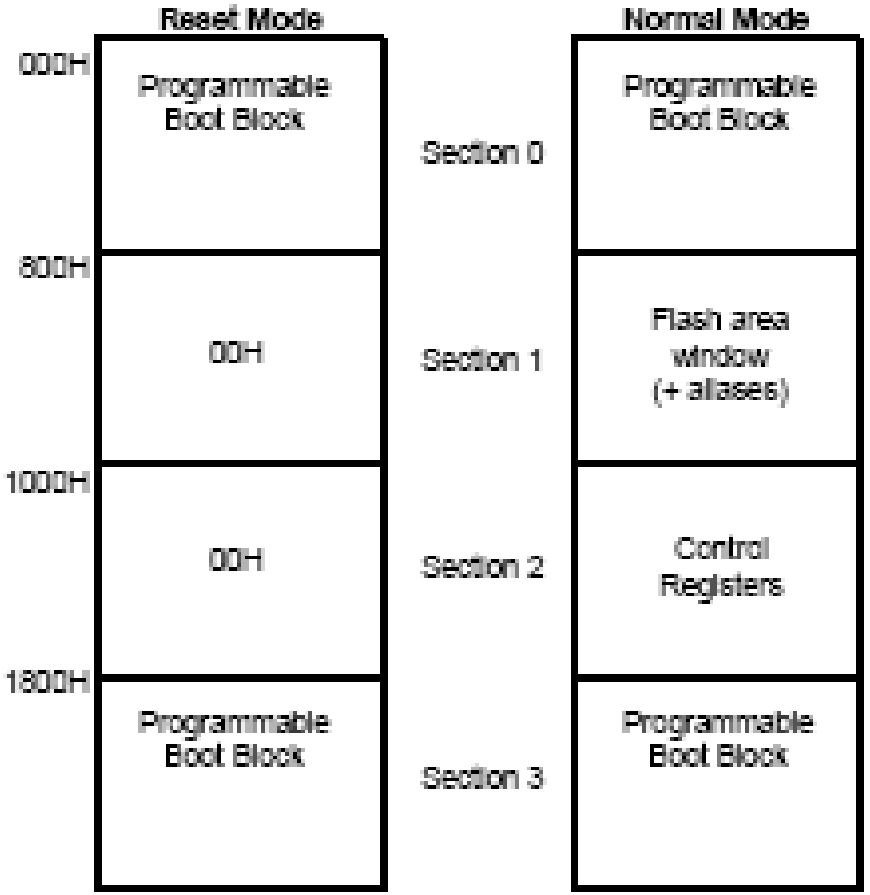


Figure 15: Mobile DiskOnChip P3 Memory Map

NEONSEVEN

Main GLOBE3 to GLOBE6 changes

Bluetooth PMB8753 on board
Audio DAC for MP3 play
Support for Memory Banking
New PA: PMB6293
New 100 pin System/Multimedia Connector
New uSD and Nand support
New GPS chip support PMB2520

Main GLOBE3 to GLOBE6 changes

The end