BP30
E-GOLDradio RF-BB Interface Specification

Edition 2006

Published by Neonseven s.r.l.,
Viale Stazione di Prosecco, 15
34010 Sgonico (Trieste) Italy

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1 Document Mission/Scope

1.1 Mission

A detailed description of RF and Base Band Interface is the mission taking in account not only the two main modules but also every single sub-block. An overview of all used signals and timing requirements has been provided to understand all interactions between Base Band the RF module, so that Customer may fit the best RF solution based on E-GOLDradio.

1.2 Scope

The scope is platform based E-GOLDradio and E-POWERlite. Inside E-GOLDradio there is a BaseBand E-GOLDlite and a transceiver SMARTi SD2 Infineon Family. For every E-GOLDradio used version, there could be a different version of SMARTi SD2 inside. The following description is generic and for every version, it's better to check the correspondent technical specification.

2 List of Acronyms

Abbreviation / Term	Explanation / Definition
BB	Base Band
AFC	Automatic Frequency Control
DCXO	Digitally Controlled Crystal Oscillator
FACCH	Fast Associated Control Channel
NTC	Negative Thermal Coefficient
FTA	Factory Test Acceptance
PA	Power Amplifier
MS	Mobile station
TCV	Timing compare value

3 Introduction

This document describes the physical interface between BB and the RF module: SMARTi SD2 GSM/EDGE 850/900/1800/1900 Voice and Data Quad-Band/Multi-Slot Transceiver, Power Amplifier and Antenna Switch. The Interface description has been divided into the following sections:

General Overview:	Describes general properties in the interface, shows the physical connections and provides information on the timing of the programming interface.
Synthesizer:	Describes the synthesizer interface.
Transmitter:	Describes the transmitter interface.
Receiver:	Describes the receiver interface.
Reference Oscillator:	Describes the interface toward master 26 MHz clock.
Power supply:	Gives some comments about power supply.
Timing	Provides information on the timing of control signals during power up and during operation.

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4 General Overview

4.1 Block Diagram

In Figure 4.1 all main sub-blocks of RF and Baseband modules are represented and all connections are highlighted:

- Four different Power Supply Voltages VRF0/1/2 and VBAT;
- 26 MHz clock provided to BB Module
- CLK, DA and EN signals for 3-wire bus used to control SMARTiSD2;
- A, AX, B, BX Interface to BB I, IX, Q and QX respectively;
- TXON_PA (T_OUT0) and PALEVEL (PAOUT1) signals used to control PA switching on/off and ramp profile;
- VC1,2,3 (T_OUT2,3,4) signals used to control Antenna switch and PA Band Switching;
- RF_TEMP used to measure the temperature of RF Module;

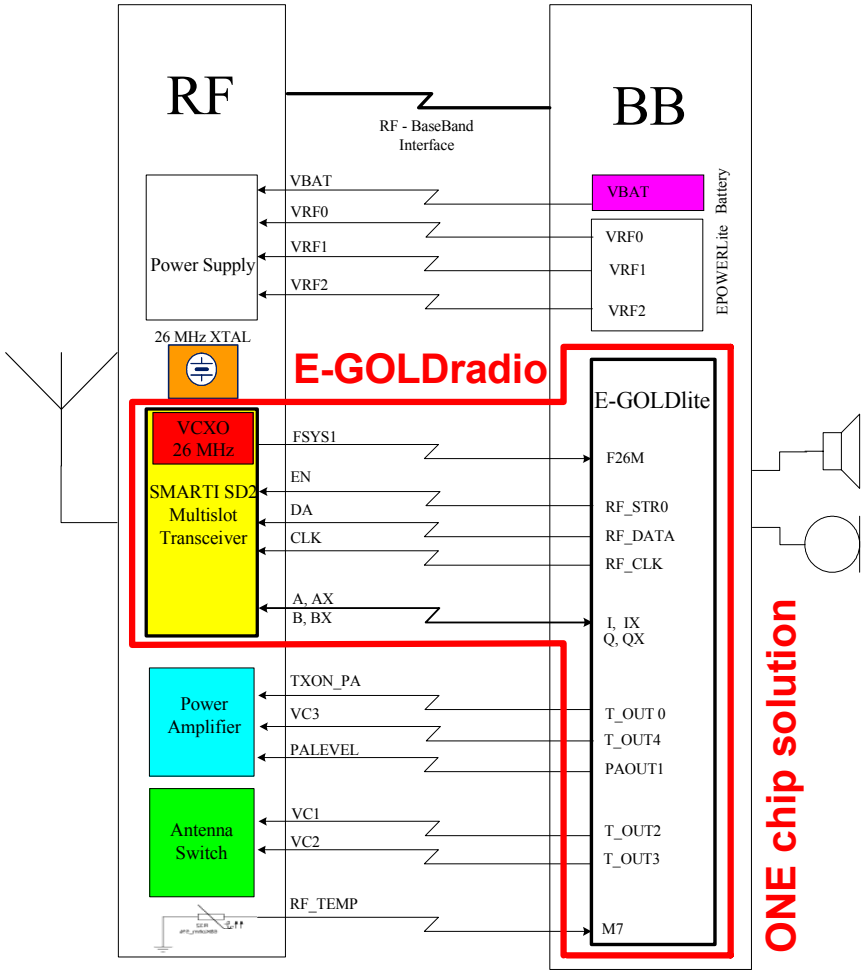

Figure 4.1 Block Diagram RF-BB Interface showing the connection

4.2 Common Programming Interface

The radio is controlled using a combination of single purpose control pins, and via a 3 wire serial bus. The 3 wire bus is used to transmit the telegrams, which are necessary to program the internal 3W control registers of the radio: Channelword1 Register (REG0), Channelword2 Register (REG1) and RX/TX Register (REG2). The description of the telegrams used to control the transceiver in different conditions (initialization after power up, AFC, receiving, transmission, switching off) will be described in the following chapters.
The bus consists of three signals:

- EN (RF_STR0)
- DA (RF_DATA)
- CLK (RF_CLK)

Please note that the three wire bus must be at 0 volts when the VRF1 is switched off.

The electrical and timing requirements for the 3 wire bus and all detailed technical notes are in the functional description of RF part inside design specification [1]. The initial revision of the chapter related to RF part is based on SMARTi SD2 target specification, Rev 2.0 [4].

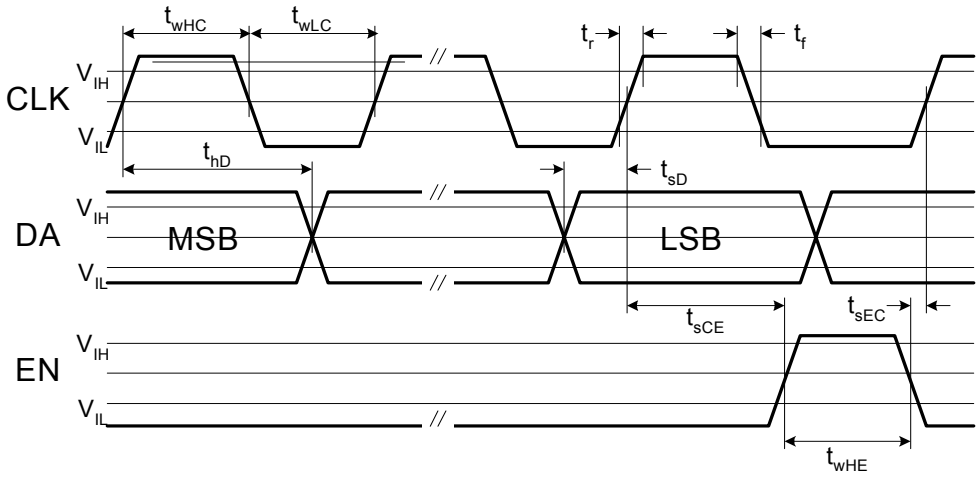

Figure 4.2: Timing of the electrical signal on the 3 wire serial interface [4]

5 Synthesizer

The SMARTi SD2 contains a fractional-N sigma-delta synthesizer for the frequency generation in the RX and TX operation mode. The reference frequency (FSYS1) is 26 MHz that is provided by the Integrated Digitally Controlled Crystal Oscillator (DCXO). FSYS1 serves as comparison frequency of the phase detector and as clock frequency of all digital circuitry [1]
Programming of the frequency synthesis in the transceiver serves several purposes. It is this programming that control the power up sequence of the transceiver (ON0, ON1 bits 15, 16 in REG1), and the programming is also used to select whether the radio is in transmit - or receive mode (TRX bit 18 in REG1). Also the synthesizer part of the band selection (850/900/1800/1900) is done using this programming (BSW0, BSW1 bits 19, 20 in REG1), i.e. this programming determines which receive/transmit path of the radio is used.

5.1 Interface Description

Two programming words are available in order to control the synthesizer:

- Channelword1 register (REG0);
- Channelword2 register (REG1);

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The first word and part of the second word are used to program the channel and the remained part of Channelword2 allows for operation mode setting: SMARTi SD2 Power Mode, Transmit/Receive mode, Band select, etc. For more detailed description of the every single bit-field, you may check in the Table 5.1 and Table 5.2 or in the document [4] for SMARTi SD2.

Bit no LSB	Value	Bit name	Function
0…3	0000	Add0/1/2/3	Register Address – CHANNEL1
4	0	F0	Frac.Channelword Part#1 bit 0
5…22		F1…F18	Frac.Channelword Part#1 bit 1…18
23 MSB		F19	Frac.Channelword Part#1 bit 19

Table 5.1 - Channelword1 register

Bit no LSB	Value	Bit name	Function
0…3	0100	Add0/1/2/3	Register Address – CHANNEL2
4	0	F20	Frac.Channelword Part#2 bit 20
5	0	F21	Frac.Channelword Part#2 bit 21
6	0	F22	Frac.Channelword Part#2 bit 22
7	0	CH0	Integer Channelword Bit 0
8	0	CH1	Integer Channelword Bit 1
9…14		CH2…CH7	Integer Channelword Bit 2…7
15		ON0	SMARTi Power Mode: 00=All off, 10=PLL test on(for test only), 01= not used, 11=ALL ON
16		ON1	
17	0		Mandatory
18		TRX	RX TX Switch RX = 0 / TX = 1
19		BSW0	Bandselect: 00 = 850, 01 = 900, 10= 1800, 11 = 1900
20		BSW1	
21	0		Mandatory
22	0		Mandatory
23 MSB	0		Mandatory

Table 5.2 Channelword2 register

Band	Freq. [MHz]	Channels	VCO freq. [MHz]	BSW0	BSW1	TRX
Tx850	824-849	128-251	3296-3396	0	0	1
Rx850	869-894	128-251	3476-3576	0	0	0
Tx900	880-915	975-1023, 0-124	3520-3660	1	0	1
Rx900	925-960	975-1023, 0-124	3700-3840	1	0	0
Tx1800	1710-1785	512-885	3420-3570	0	1	1
Rx1800	1805-1880	512-885	3610-3760	0	1	0
Tx1900	1850-1910	512-810	3700-3820	1	1	1
Rx1900	1930-1990	512-810	3860-3980	1	1	0

Table 5.3 Programming of VCO bands.

The RX/TX path selection, and LO RF-VCO band switch selection bits are programmed according to Table 5.3.

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5.2 Programming of the Fractional-N SIGMA-DELTA [4]

Fractional-N frequency synthesis allows the use of higher phase detector frequencies than the desired channel spacing. Especially with Sigma-Delta fractional-N frequency synthesizers the frequency resolution can be increased to a few Hz and therefore the GSM system specification can be fulfilled. On the other hand the crystal reference can be used as phase detector frequency. The advantage is a resulting smaller divider ratio of the phase-locked loop and therefore an improvement of the phase noise performance.
The frequency of the internal VCO is controlled by two 24 bit registers i.e. Frac.Channelword Part#1 for the lower 20 bits (F19-F0) of the fractional part (**NF**) and Frac.Channelword Part#2 for the 3 MSBs (F22-F20) of the fractional part (NF) and 8 bits (CH7-CH0) of the integer part (**NI**) of the divide ratio. Both values form the fractional channel word **CW**:

$$CW = NI \bullet NF$$

The internal VCO frequency (f_{VCO}) is given by:

$$f_{VCO} = NI \bullet NF \bullet f_{PD}$$

Respectively

$$f_{VCO} = \left(NI + \frac{NF}{MOD} \right) \bullet f_{PD} \qquad MOD = 2^{Aw} = 2^{23} = 8388608$$

For the SMARTi SD2 the phase detector frequency f_{PD} is 26 MHz (FSYS1) and the fractional modulus MOD is given by the accumulator width Aw (23 bits) of the Sigma-Delta-MASH modulator:
In SMARTi SD2 Specification [4] you may find an example of the complete calculation of the integer and fractional part of the divide ratio, in the present document the final equations follow:

$$NI = floor\left(\frac{D \bullet f_{CH}}{f_{PD}} \right) \qquad \frac{NF}{MOD} = \frac{f_{CH} \bullet D - NI \bullet f_{PD}}{f_{PD}}$$

6 Transmitter

In order to perform a TX burst BB module should transmit a sequence of telegrams to the transceiver and at the right time activate all necessary signals to control the power amplifier and antenna switch module.
All details and the requested timing sequence will be described in the following paragraph. In the next paragraphs will be described the contents of RX/TX Register (REG2), the antenna switch control, power ramping and calibration, TX compensation applied, timing adjustment and finally multislot intermediate ramps.

6.1 TX telegrams, signals and timing requirements

In GSM System Interface two groups are available in order to perform a TX burst: TX ON and TX OFF groups. Every group activates a set of events that control the BaseBand Part and the RF module at the same time.
The active signals in TX ON Group are represented in the
Figure 6.1 and all timing requirements are highlighted; the E-GOLDlite internal signals are [1]:

- CODON signal enables the digital part of modulator and it should be set before TXON.
- TXON should be set after CODON in order to enable the analog blocks of the PA power ramping HW as well.

The BB-RF signals are:

- 3 telegrams should be transmitted, first two used to program the synthesizer (frequency setting) and the last one only to trigger the internal modulator; the first two telegrams are transmitted using the Multiple Telegram Transmission Control (Burst Mode) supported by RF Control Unit of E-GOLDlite. The third telegram programs the internal RX/TX register REG2; a detailed description on its content is in the next paragraph. The time interval between the transmission of the second and the beginning of tx burst

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SHALL satisfy the timing requirement of the used transceiver (for SMARTi SD2 a typical value = 150 μs and max value = 220 μs are guaranteed)[1]. Furthermore time interval between the setting of CODON signal and the starting transmission of RX/TX REG2 telegram SHALL BE around 50 μs and 21 dummy symbols used.

- PRx Power Ramp Up signal used to trigger the starting time of Power Ramp x located at the x position inside RF RAM; note that there is a delay (> 20 obit) between setting of PRx and starting of Ramp up.
- VC1/2/3 (T_OUT2/3/4) are the signals used to control the antenna switch and band switch of PA, all output configurations are represented inTable 6.2.
- TXON_PA and PAOUT1 used respectively to switch ON/OFF power amplifier and to program the power ramp profile. Only the last M (M value depends by the used PA, see Annex 1) ramp steps after the PA switching on are useful and enough to determine the output power ramp up profile.

The active signals in TX OFF Group are represented in the Figure 6.2 and all timing requirements are highlighted; the E-GOLDlite internal signals are [1]:

- TXON has to be always switched off before CODON in order to disable the modulator in a correct way.

The BB-RF signals are:

- Only one telegram should be transmitted to switch off transceiver; only REG1 should be programmed to switch off.
- PRx Power Ramp Down signal used to trigger the starting time of Power Ramp x located at the x position inside RF RAM; note that there is a delay (> 20 obit) between setting of PRx and starting of Ramp down.
- The antenna switch is switched off after step N (N value depends by the used PA, see Annex 1) of ramp down.
- Only the N ramp steps before the PA switching off are useful and enough to determine the output power ramp down.

6.2 RX/TX Register (REG2)

6.2.1 RX/TX Register (REG2) for TX burst

For tx burst generation, RX/TX register (REG2) is useful only to start the internal modulator and all info bits are zeros.

The programming word is shown in the Table 6.1.

Bit no LSB	**Value**	**Bit name**	**Function**
0…3	0010	Add0…3	Register Address RXTX
4	See	RXGAIN	
5	See	RXGAIN	RXGAIN allows to select 57/43/23 dB input LNA gain
6	See	RXCORR0	RXCORR[3:0] allows to compensate minor process and temperature changes; range[-6dB,+6dB], step 1dB
7	See	RXCORR1	
8		RXCORR2	
9		RXCORR3	
10	0		Mandatory
11		RXCM0	RX-Out Common Mode Level 00 = 0.95V / 01=1.25V / 10=1.35V / 11=1.425V
12		RXCM1	
13…16		RXGS0…3	RXGS allows -6 dB to +18 dB in 3 dB step output gain
17		OFC	DC Offset Compensation = 0 OFF
18…23	0		Mandatory all zeros

Table 6.1 RX/TX register [2]

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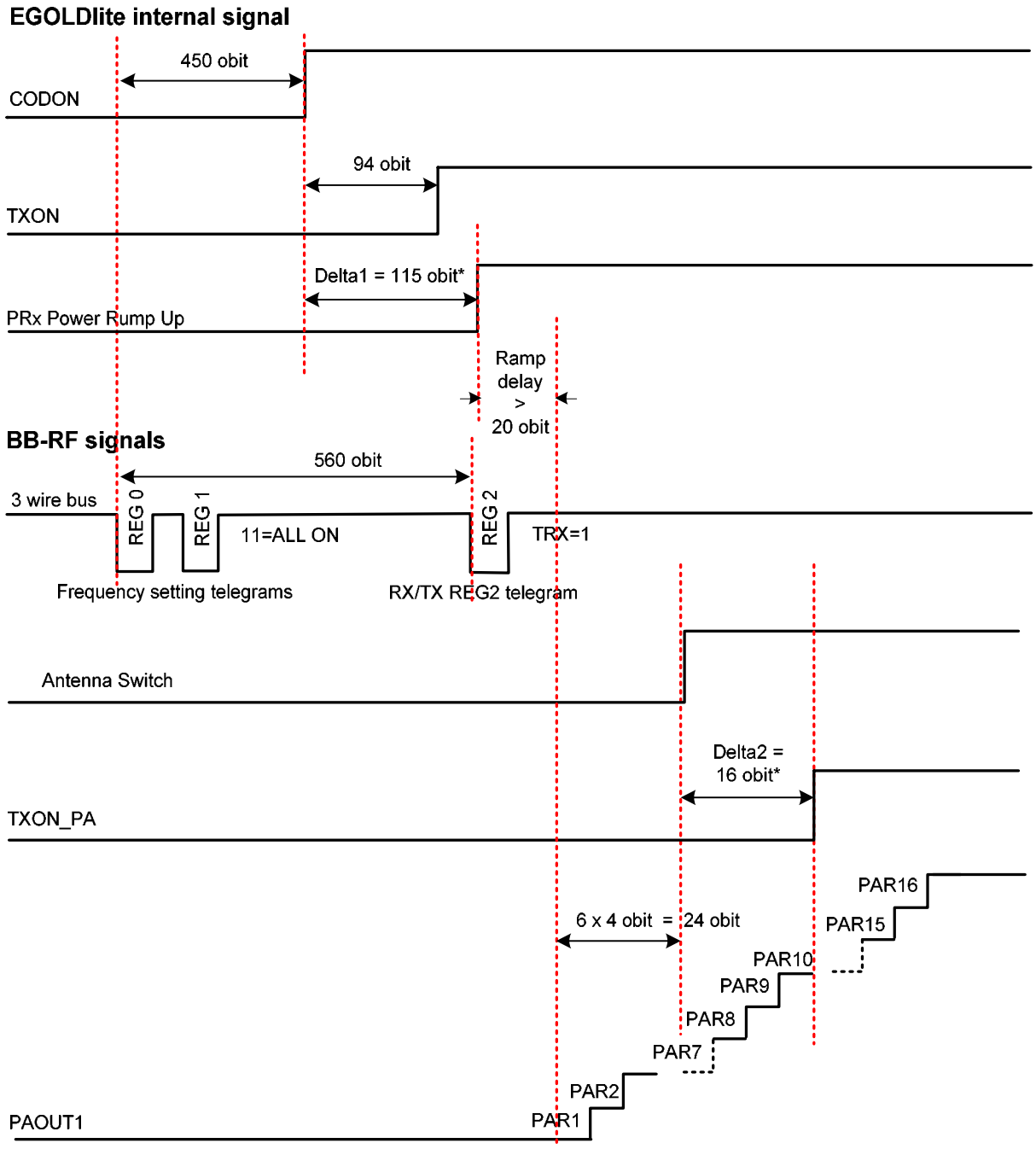
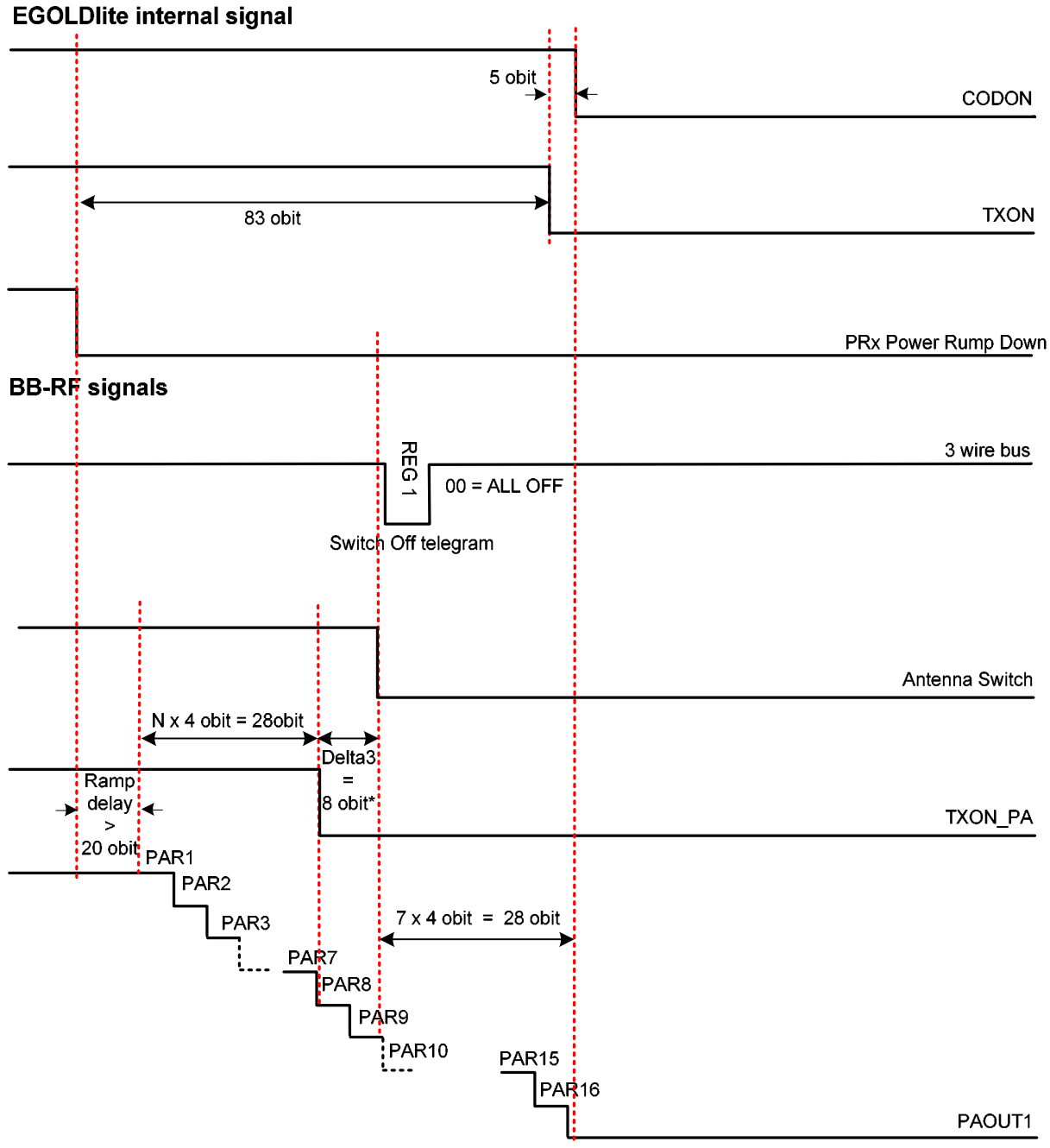
Signal Timing for TX ON Group



TIME SCALE: octalbit (1 obit = 1/8 bit = 0,46 µs)
All timing values marked with * are PA dependent, see Annex 1.

Figure 6.1 Active Signals in TX ON Group

Signal Timing for TX OFF Group



TIME SCALE: octalbit (1 obit = 1/8 bit = 0,46 µs)
All timing values marked with * are PA dependent, see Annex 1.

Figure 6.2 Active Signals in TX OFF Group

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6.3 Antenna switch control

The control of the antenna switch defined in Table 6.2 is only indicative. In any case you should refer the technical note of used antenna switch.

VC1	VC2	Description Switch Mode
0	0	EGSM RX
1	0	EGSM TX
0	1	PCS/DCS TX
0	0	PCS/DCS RX

Table 6.2 Logic levels for control of antenna switch.

6.4 I/Q Swapping.

No I/Q swapping are required.

6.5 Power Ramping and Calibration

This section contains information about the 32 (= 2 x 16) ramp control values for ramping up and down as well as information about offset, channel and temperature compensation.
The applied max power level PACT[16], that sets the output RF power during the useful part of the burst, is the result of a default level value plus all compensation values. The number of compensative addends depends by the features RF_GENERIC_INTERFACE and ANTENNA_DETECTION:

```
#if defined (ANTENNA_DETECTION) && defined (RF_GENERIC_INTERFACE)
PACT[16]  =  Default_Level_XX[16]
                                + eep_static.rf_adjcomp.pa_offset[x][x]
                                + eep_static.rf_tx_comp.pa_ch_comp[x][RF_get_ch_comp_index]
                                + eep_static.rf_comp.pa_temp_comp
                                + gsm.pl_vcc_offset
                                + eep_static.rf_tx_comp.antenna_ch_comp[x][RF_get_ch_comp_index]
#else
PACT[16]  =  Default_Level_XX[16]
                                + eep_static.rf_adjcomp.pa_offset[x][x]
                                + eep_static.rf_comp.pa_ch_comp[x][RF_get_ch_comp_index]
                                + eep_static.rf_comp.pa_temp_comp
                                + gsm.pl_vcc_offset
#endif
```

The [x][x] above indicates the band and the power level. The detailed information about how to adjust the TX is described in the ATE#2 [5]. An overview of all Eeprom parameters can be seen in the EEP.C file.

6.5.1 Default Power Ramp Table

There is one different default table for every frequency band XX (= GSM850, EGSM900, DCS1800 and PCS1900): Default_Level_XX[1..16] are the up ramp values for power level x, Default_Level_XX[17..32] are the down ramp values for power level x. Default_Level_XX[16] is the max power level of the ramp up and correspond to the default power level of Tx burst. The tables are scaled to fit control values in the range 0 to 2047. The ramps are not stored in the Eeprom section of the flash, but are defined constant tables in the code. Every single value can only be adjusted from the phonetool in inline mode.

6.5.2 Power Level Calibration

The applied offset values are calculated from measurements in production and saved in EEPROM. The offset values should be added to the last parameter in the ramp up, and there is a value for each power level:

Eep_static.rf_adjcomp.pa_offset[x][0..19]

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The first parameter x indicates the selected band. Take care that different band configurations support different index associated to a single band, for example European Dual Band EGSM900 = 0, DCS1800 = 1 and Quad Band GSM850 = 0, EGSM900 = 1, DCS1800 = 2 and PCS1900 = 3. The lower band is always associated to the lower index.

6.5.3 TX Channel Compensation

The TX channel compensation can be made mainly to compensate for ripple in the transmit output path. The channel compensation is only necessary for maximum power level supported by the mobile, while these levels have the closest tolerances. One table for each band supported by the mobile are necessary. In the Table 6.3 there are the intervals in which are divided the different Bands. All default values without calibration are zeros.

The parameter should be a delta value, which has to be added to the last value in the up ramp.

GSM850	EGSM900	GSM1800	PCS1900	EEprom name
128 to 152	0 to 25	512 to 600	512 to 600	Eep_static.rf_comp.pa_ch_comp[x][0]
153 to 226	26 to 99	601 to 700	601 to 700	Eep_static.rf_comp.pa_ch_comp[x][1]
226 to 251	100 to 124	701 to 800	701 to 800	Eep_static.rf_comp.pa_ch_comp[x][2]
-	975 to 1023	801 to 885	801 to 885	Eep_static.rf_comp.pa_ch_comp[x][4]

Table 6.3 TX-channel compensation. Only valid at +25°C.

When the features RF_GENERIC_INTERFACE and ANTENNA_DETECTION are active, Eep_static.rf_comp.pa_ch_comp[x][x] is replaced by Eep_static.rf_tx_comp.pa_ch_comp[x][x]. Furthermore if MS uses the internal antenna, there is the other addend Eep_static.rf_tx_comp.antenna_ch_comp, which compensates the effect of board-by-board channel calibration (for External Antenna).
The future RF_GENERIC_INTERFACE allows setting the correspondent compensation value for a maximum of ten intervals for each band supported.

6.5.4 TX Temperature Compensation

The TX temperature compensation can be made in five temperature ranges to compensate for tolerances in the PAOUT1 DAC and Power Amplifier. The temperature compensation is stored in EEPROM, but can be fixed on all units and need no production measurement. The exact values will be determined on the last pre series before FTA. The values in the table are examples only. Maximum four tables are necessary, one for each band support by the SW.

The compensation of the TX PA can be based on an allowed temperature error of max. 10°C. The temperature rises due to transmitting is approx. 1°C per minute that allows maximum 10 minutes between the necessary temperature corrections. However, due to other tolerances an update for each FACCH is recommended.

The temperature compensation is done only on the highest power levels (GSM850, EGSM900: 5, GSM1800, PCS1900: 0).

Actually for BP30 the default temperature compensation values applied are zeros and the temperature ranges are represented in Table 6.4.

Temperature [°C]	EEprom name
-30 to –11	eep_static.rf_comp.pa_temp_comp[x][0]
-10 to +9	eep_static.rf_comp.pa_temp_comp[x][1]
+10 to +29	eep_static.rf_comp.pa_temp_comp[x][2]
+30 to +49	eep_static.rf_comp.pa_temp_comp[x][3]
+50 to +69	eep_static.rf_comp.pa_temp_comp[x][4]

Table 6.4 Default TX temperature compensation values.

The parameter should be a delta value, which has to be added to the last value in the up ramp.

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6.5.5 TX Supply voltage compensation

The TX supply voltage compensation has to lower the output power when the supply voltage (CHR_RF_MEAN_VCC measured inside tx burst) is below a threshold value. The compensation is only active at max power level. The delta to PACT[16] should be calculated as:

$$offset\_step * (threshold - CHR\_RF\_MEAN\_VCC)$$

The parameters are:

eep_static.rf_comp.pa_vcc_comp[x].threshold	33
eep_static.rf_comp.pa_vcc_comp[x].offset_step	10

The threshold value has to be Vcc*10 i.e. 3.3V is stored as 33. There should be a set of parameters for each band supported by the MS. By setting the offset step is possible to define the corrective delta value to be added to last power up value for each 100 mV variation in supply voltage.

6.5.6 Timing Adjustment

The starting time of the power ramp up and down of the Tx burst could be adjusted for different frequency band and power level value setting the correspondent values in eep:

- eep_static.rf_adjcomp.pa_timing_offset[x][0..19].rampup;
- eep_static.rf_adjcomp.pa_timing_offset[x][0..19].rampdown;

Actually on BP30 platform their default values are zeros. These values could be changed, but the applied time adjustment to start the ramp up MUST be inside the allowed range, that depends by the used PA (see Annex 1). In any case the fine tuning of power ramp profile should be enough to fulfill completely the RF requirements. Only for PA Axiom these entries are used to apply a different TCV to set and reset TXON_PA respectively.

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6.6 *Multi slot intermediate ramp*

An intermediate ramp has to be generated to support GPRS multi slot class 10 (2 max. uplink timeslots). The 16 values of intermediate power ramp are calculated starting from the values of both ramps up and down:

- The first five steps of intermediate ramp are always equal to the power hold value of first tx timeslot.
- The six middle steps are calculated using the step values of ramp up and down in the following way; when the power level of second tx timeslot is minor than first one, step by step the intermediate ramp will be programmed with the power hold value of the first one until the compared value of the second slot is grater (see Table 6.5: in the example intermediate ramp values are calculated without taking account of RF compensation). In the other case when the power level of the first timeslot is minor than second one, for the six intermediate ramp steps will be used the steps of ramp down until their values are grater than the hold power value of second tx slot (see Table 6.6). Furthermore when the power level of both tx timeslots are the same, all values of intermediate ramp are equal to the power hold value of first timeslot.
- The last five steps of the intermediate ramp are always equal to the power hold value of the second timeslot.

Down Ramp TS1	Hold value 340	320	250	200	180	150	50	50	50	50	50	50	50	50	50	50	50
Up Ramp TS 2	Hold value 750	50	50	50	50	50	50	50	50	50	150	180	280	400	500	650	750
Inter. Ramp	-	340	340	340	340	340	340	340	400	500	650	750	750	750	750	750	750

Table 6.5 Intermediate ramp values between tx ts with power level 13 and 8 respectively (EGSM 900).

Down Ramp TS1	Hold value 750	660	500	320	200	170	50	50	50	50	50	50	50	50	50	50	50
Up Ramp TS 2	Hold value 340	50	50	50	50	50	50	50	50	50	140	150	150	220	300	320	340
Inter. Ramp	-	750	750	750	750	750	660	500	340	340	340	340	340	340	340	340	340

Table 6.6 Intermediate ramp values between tx ts with power level 8 and 13 respectively (EGSM 900).

The power hold values used to calculate the intermediate ramp are the values of default tables already corrected with the delta added by RF compensation. The starting timing of the intermediate ramp is fixed because there is no need to change it: the first 6 (6 * 4 = 24 obit) and last 6 steps of intermediate ramp equal to the power hold values of two tx timeslot should be an enough guard time to avoid outside of power mask during the ramp transition.

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7 Receiver

Equalizer, SMARTi SD2 Transceiver and antenna switch shall be controlled to open an RX window; all signals used to perform it are described following in detail. After RX timing requirements, there is a description about the setting of RX path internal to SMARTi SD2 that is programmed by RX/TX Register telegram. At the end of chapter RX Calibration is just introduced.

7.1 RX telegrams, signals and timing requirements

In GSM System Interface two groups are available in order to perform the RX burst: RX ON and RX OFF groups. Every group activates a set of events that control the BaseBand Part and the RF module at the same time.

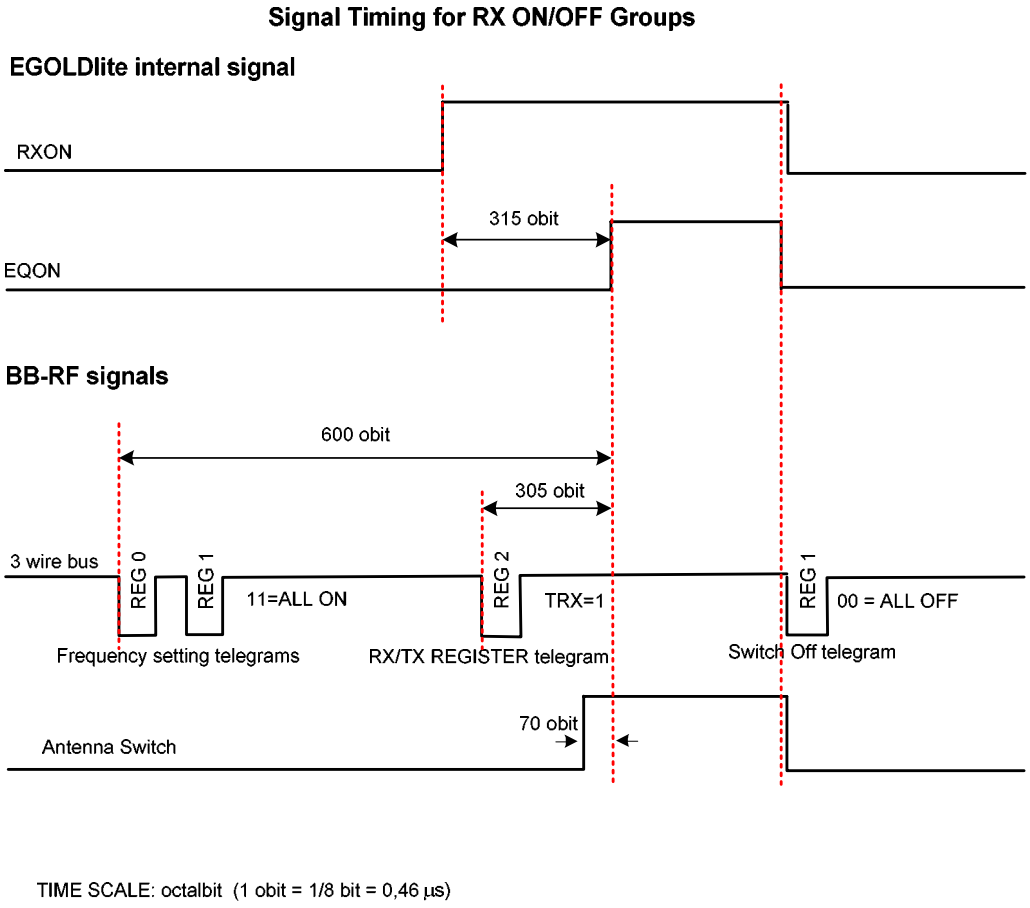

Figure 7.1 Signal Timing for RX Window

The active signals are represented in the Figure 7.1 and all timing requirements are highlighted; the E-GOLDlite internal signals are [1]:

- EQON signal enables the digital part of equalizer.
- RXON must be set about 130 µs before the rising edge of EQON, FCON, MONON or SCON; in fact the analog part and BB-filter are stable only about 130 µs after setting RXON. The samples written before that time are not valid.

The BB-RF signals are:
3 telegrams should be transmitted, first two used to program the synthesizer (frequency setting) and the last one to program RX Gain path; the first two telegrams are transmitted using the Multiple Telegram Transmission Control (Burst Mode) supported by RF Control Unit of E-GOLDlite. The third telegram programs the internal

RX/TX register REG2; a detailed description on its content is in the next paragraph. The time interval between the transmission of the second and the starting time of RX burst shall be more than 220 µs; furthermore the last telegram shall be transmitted more than 136,5 µs (**100µs** + 32 µs + 4,5 µs) before the Rx window in order to avoid a residual DC offset drift.The timing requirement of **100µs** between rising enable of REG2 and the active RX burst is recommended by specification [1]. The recorder data during EQON/MONON are available 32 µs after the data input on the IQ Interface due to the delay of the harware filter inside Base Band of E-GOLDlite. Take in account also 4,5 µs the time needed to transmit telegram.

- VC1/2 (T_OUT2/3) are the signals used to control the antenna switch, the different output configuration is represented in Table 6.2.

7.2 RX/TX Register (REG2) for Rx window [4] [1]

The RX/TX Register is used to control the internal RX path of SMARTi SD2 that it could be divided in the following main parts:

- **RF front-end.** The receiver contains all active circuits for a complete receiver chain. The GSM850/900/1800/1900 **LNAs** with balanced inputs are fully integrated. No interstage filtering is needed. A programmable gain step is implemented (**RXGAIN**).
- **Demodulator and Baseband Stage.** The amplified RF-signal is direct converted by a quadrature demodulator to the final output signals at the baseband frequency. The orthogonal LO signals are generated by a divider by four for GSM850/900 band and a divider by two for the GSM1800/1900 band. The resulting in-phase and quadrature signals are fed into the baseband stage that comprises a low pass filtering, a programmable gain step (**RXGS**) and a programmable gain correction stage (**PGC**). The baseband filters provide sufficient suppression of blocking signals and adjacent channel interferers to fit into baseband ADC's providing 72dB dynamic range at full scales from 1Vpp to 4Vpp. The ADC's anti-aliasing requirements are fulfilled for sampling rates from 6.5MHz on. The PGC provides a gain correction range from -6dB to +6dB in 1dB steps. The additional gain step (**RXGS**) is recommended to minimize the baseband ADC noise contribution for wanted signal levels Pw<-90dBm at the antenna input.

Only three RX GAIN levels are used and the values with the correspondent RX Gain Bit Setting that are used to program RX/TX Register (REG2) are written in theTable 7.1

RX Gain level [dB]	RXCORR value = 0dB – PGC	RXGAIN LNA	RXGS
22	0010	00	0000
57	0010	11	0000
63	0010	11	0010

Table 7.1 Rx Gain Bit Setting

The RXCORR field is only used to apply the RX gain correction for RF compensation; there are three different contributions and every single correction value is described in the next paragraph:

- Channel compensation;
- Gain compensation;
- Temperature compensation;

7.3 I/Q Swapping.

No I/Q swapping are required.

7.4 RX Calibration

The detailed information about Rx calibration is described in the ATE#2 [5]. An overview of all EEPROM parameters can be seen in the eep.c file.

7.4.1 RX gain vs. channel calibration

The RX path might be calibrated in six sub-bands for GSM850, EGSM900 and eight sub-bands for GSM1800, PSC1900 to compensate for tolerances in the receive filters. The RX gain vs. channel compensation might be done in the production tester. The EEprom parameter names and the sub-bands frequency boundaries are given in **Table 7.2**, **Table 7.3**, **Table 7.4** and **Table 7.5**, all default delta values are zeros. The RX channel compensation is calibrated at +25°C.

RX channel	EEprom name
128 to 147	eep_static.rf_adjcomp.rxlev_ch_comp[0][0]
148 to 167	eep_static.rf_adjcomp.rxlev_ch_comp[0][1]
168 to 187	eep_static.rf_adjcomp.rxlev_ch_comp[0][2]
188 to 207	eep_static.rf_adjcomp.rxlev_ch_comp[0][3]
208 to 227	eep_static.rf_adjcomp.rxlev_ch_comp[0][4]
228 to 251	eep_static.rf_adjcomp.rxlev_ch_comp[0][5]

Table 7.2 RX-channel calibration for GSM850.

RX channel	EEprom name
0 to 25	eep_static.rf_adjcomp.rxlev_ch_comp[1][0]
26 to 50	eep_static.rf_adjcomp.rxlev_ch_comp[1][1]
51 to 75	eep_static.rf_adjcomp.rxlev_ch_comp[1][2]
76 to 100	eep_static.rf_adjcomp.rxlev_ch_comp[1][3]
101 to 124	eep_static.rf_adjcomp.rxlev_ch_comp[1][4]
975 to 1023	eep_static.rf_adjcomp.rxlev_ch_comp[1][5]

Table 7.3 RX-channel calibration for EGSM900.

RX channel	EEprom name
512 to 550	eep_static.rf_adjcomp.rxlev_ch_comp[2][0]
551 to 600	eep_static.rf_adjcomp.rxlev_ch_comp[2][1]
601 to 650	eep_static.rf_adjcomp.rxlev_ch_comp[2][2]
651 to 700	eep_static.rf_adjcomp.rxlev_ch_comp[2][3]
701 to 750	eep_static.rf_adjcomp.rxlev_ch_comp[2][4]
751 to 800	eep_static.rf_adjcomp.rxlev_ch_comp[2][5]
801 to 850	eep_static.rf_adjcomp.rxlev_ch_comp[2][6]
851 to 885	eep_static.rf_adjcomp.rxlev_ch_comp[2][7]

Table 7.4 RX-channel calibration for GSM1800.

RX channel	EEprom name
512 to 550	eep_static.rf_adjcomp.rxlev_ch_comp[3][0]
551 to 590	eep_static.rf_adjcomp.rxlev_ch_comp[3][1]
591 to 630	eep_static.rf_adjcomp.rxlev_ch_comp[3][2]
631 to 670	eep_static.rf_adjcomp.rxlev_ch_comp[3][3]
671 to 710	eep_static.rf_adjcomp.rxlev_ch_comp[3][4]
711 to 750	eep_static.rf_adjcomp.rxlev_ch_comp[3][5]
751 to 790	eep_static.rf_adjcomp.rxlev_ch_comp[3][6]
791 to 810	eep_static.rf_adjcomp.rxlev_ch_comp[3][7]

Table 7.5 RX-channel calibration for PCS1900.

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7.4.2 RX level linearity calibration

Rx Gain linearity must be calibrated to compensate for tolerances on the biggest gain steps. This has to be done in the production tester. The mobile is tested at least at two different input levels per band: one should be performed using low Rx Gain (LNA off) setting and the other with high when LNA is switched on (e.g. at RF input levels of -48dBm and -75dBm respectively). Input levels are the suggested test levels in production for both all bands. The measured values are then used to calculate the compensation values (one for each input level), which should be entered in EEprom. The EEprom parameter name is:

eep_static.rf_adjcomp.rxlev_gain_comp[x][0..69]

where the first parameter x indicates the selected band. (x = 0 for GSM850, 1 for EGSM900, 2 for GSM1800, and 3 for PCS1900) and the second parameter refers to the input level (0 for –110 and 69 for –40)

RX gain is calibrated at +25°C at channel 189 for GSM850, 37 for EGSM900, 699 for GSM1800 and channel 661 for PCS1900.See ATE#2 [5] for details.

7.4.3 Rx temperature compensation

RX Temperature compensation is adjusted in five temperature ranges to compensate for temperature dependencies in the receive filters and gain stages. The temperature compensation is to be fixed on all units and need no production measurement. The exact delta values must be determined on the last pre series before FTA.

The first parameter in the name indicates the band (0 for GSM850, 1 for EGSM900, 2 for GSM1800, and 3 for PCS1900).

Note: Temperature calibration will be performed at channel 189 for GSM850, 37 for EGSM900, 699 for GSM1800 and channel 661 for PCS1900.

Temperature [°C]	EEprom name
-30 to –11	eep_static.rf_comp.rxlev_temp_comp[0..3][0]
-10 to +9	eep_static.rf_comp.rxlev_temp_comp[0..3][1]
+10 to +29	eep_static.rf_comp.rxlev_temp_comp[0..3][2]
+30 to +49	eep_static.rf_comp.rxlev_temp_comp[0..3][3]
+50 to +69	eep_static.rf_comp.rxlev_temp_comp[0..3][4]

Table 7.6 Example of EGSM900 temperature compensation.

8 Transceiver Initialization

If the mobile station has been switched off or entering in power saving, the VRF1 voltage has been removed and SMARTi SD2 comes to an undefined state. After power on of mobile or after exit from power saving, the transceiver before to perform an RX or TX window has to be initialize transmitting a sequence of initialization and XO_INITx telegrams. The contents and the number of these telegrams are described in the correspondent specification [4].

9 Temperature Sensor

The temperature sensor is a NTC thermistor that is connected to M7 measurement input of E-GOLDlite. It will be useful to perform temperature measurement used for temperature compensation of the RF. Actually this external temperature sensor isn't used and only on-chip temperature measurement is performed. We assume that the temperature of E-GOLDlite and transceiver is the same. The temperature sensor for measurement of the on chip temperature (TIC) is placed in the mixed signal section of the chip in the neighborhood of the controller block. The temperature characteristic of a well-defined semiconductor junction at a defined current level is used for determining the on chip temperature [1].

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10 Reference Oscillator

On E-GOLDradio based platform the reference oscillator in use is the Integrated Digitally Controlled Crystal Oscillator **DCXO** of SMARTi SD2.

10.1 Interface Signals

The reference oscillator uses the following signals:

- FSYS1: Output 26MHz signal.
- 3 wire serial bus: DCXO initialization telegrams should be transmitted to program internal register XO_INIT1/2/3 and AFC telegram to program XO_TUNE register.

10.2 Interface Description

SMARTi SD2 offers 3 auxiliary clock outputs:

- FSYS1 is the main system clock 26MHz
- FSYS2 and FSYS3 buffered 26 MHz outputs for subsystem clocks (display, MIDI, bluetooth, companion chips, etc.). On BP30 FSYS3 is used by bluetooth.

DCXO includes an AFC plus a linearization LUXO© circuitry.
LUXO© can be disabled, so 17-bit AFC direct control of capacitor array is possible. On BP30 platform LUXO© is active (normal usage) and 8 possible subranges (bits XO_INIT1.XOCAL1..3 in XO_INIT1 register) can be selected programming XOCAL. In this case 13-bit AFC is available.
For any details of the info bit fields in these internal registers you may check in the technical specification [4].

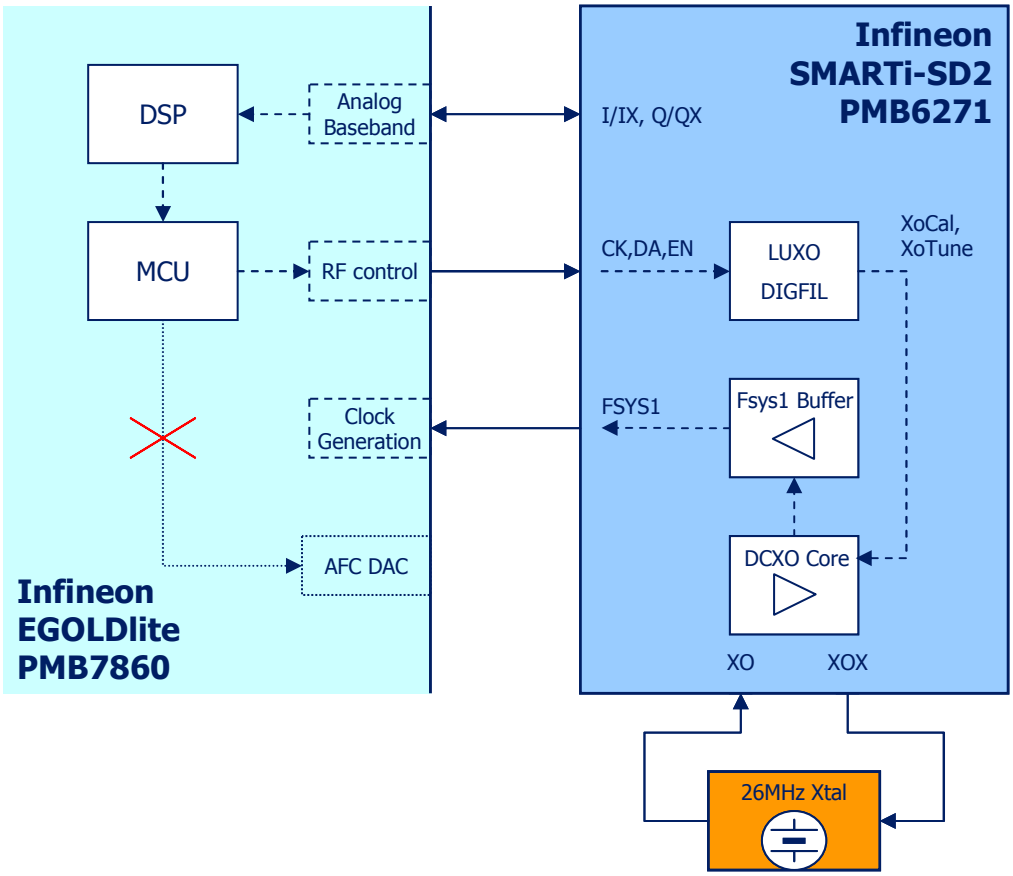

Figure 10.1 DCXO and LUXO© Circuitry

After power up and wake-up exiting from power saving all DCXO initialization and AFC telegrams should be transmitted. AFC telegram will be also transmitted every time that the mobile station needs to correct frequency. It depends by the AFC algorithm used in the software.
The AFC middle position and the AFC slope values that could be changed in EEPROM are:

- eep_static.rf_adjcomp.afc.default_dac_value = (4U << 13)|(3333U << 0) Default DAC value for 8pF XO.
- eep_static.rf_adjcomp.afc.dac_step_gsm_in_hz = 7.

The calibration procedure, used to determine the two previous values, is described in ATE#2 [5] documentation.

10.3 The DCXO SW Algorithms

10.3.1 Initial locking, FB search

Using the values of aging and frequency stability of XO used, the initial frequency error after turn-on of the mobile at any temperature (measured on a calibrated phone: default_dac_value stored in the Eeprom) could be calculated. We may suppose to use a XO that it's as high as ± 11.0 ppm (Aging 10 + frequency stability). This means that the frequency error when receiving at PCS1900 could be worst case ±22 kHz. If the phone however is turned on at the same temperature as the temperature at the calibration time, then the frequency error could be maximum ± 1 ppm (Aging 1 year) or ±1kHz at PCS1900. For GSM900 the frequency errors will be the half.
For E-GOLDlite the maximum deviation between carrier frequencies of mobile and base station which can be measured is ±15 kHz in normal conditions. In ideal conditions (GSM tester) the range for a successful FCB search is ±25 kHz**,** but this value cannot be guaranteed under real conditions [3]. In any case both values are greater than max frequency error, so that no special search procedure will be necessary.

11 Power Supply

VRF0 (VRFC on E-POWERlite), VRF1 (VRF1 on E-POWERlite) and VRF2 (VRF2 on E-POWERlite) are generated by the E-POWERlite IC in the base band. VRF2 only supplies the DCXO (system clock). The ranges of these supply values are in the Table 11.1.

		Min	Nom	Max	
VBAT	V_{BAT}	3.0	3.8	4.1	V
VRF0	VRF0	1.40	1.50	1.60	V
VRF1	VRF1	2.40	2.50	2.60	V
VRF2	VRF2	2.40	2.50	2.60	V

Table 11.1 Supply values used by RF module [2]

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References

11.1 External

[1] Infineon, “E-GOLDradio PMB 7870 GSM/GPRS Single Chip Solution”, Design Specification, Rev. 1.05, 2005-08-02.
[2] Infineon, “PMB6814 V1.0 E-POWERlite”, Target Specification, Rev. 3.2, 2004-07-04.
[3] Infineon, “E-GOLDradio PMB 7870 GSM/GPRS Single Chip Solution”, Firmware Manual, Rev. 1.04, June 2005.
[4] Infineon, “PMB 6271 GSM/EDGE 850/900/1800/1900 Voice and Data Quad-Band/Multi-Slot Transceiver”, Specification, Rev 2.0.

11.2 Internal

Title	Doc ID
[5] ATE#2 adjustment Specification	BH03.S2.TS.000005

12 Document change report

	Change Reference		Record of changes made to previous released version	
Rev	**Date**	**CR**	**Section**	**Comment**
1.0	09/01/2006	NA	Document created	First version for E-GOLDradio.

13 Approval

Revision	Approver(s)	Date	Source/signature
1.0	Stefano Godeas	13.01.2006	Document stored on server

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14 Annex 1

14.1 PA dependent timing constrains

There are different timing constrains for each PA used as described in the following **Table 14.1**:

PA	Delta1	Delta2	Delta3	M	N
Infineon PMB6293	111	16	8	7	7
Agilent AGPM7863	115	6	1	9	9

Table 14.1 Timing Constrains for different PA

Delta1 and Delta2 are the timing constrains related to the ramp up profile of TX ON group (see Figure 6.1); Delta3 is related to time interval between resetting of TXON_PA and Antenna Switch signals in TX OFF group (see Figure 6.2). M and N are respectively the number of useful steps to delineate the power ramp profiles of up and down. Take care that the M value could be affected by the used type of antenna switch (check its internal delay).
About timing adjustment there are two different usages of pa_timing_offset rampup/down applied values:

1. for PA TriQuint and Agilent they could be used to change the starting time of ramp up and down;
2. Only for Infineon PMB6293 they are used to change the starting time of setting and resetting TXON_PA signal.

In the next table you may find the allowed range of timing offset adjustment for the different PA actually supported. Take care that the right and useful adjustment should be maximum +/- 16 obit, it should be useful only to perform a fine tuning.

PA	PA timing offset ramp up Allowed range	PA timing offset ramp down Allowed Range
Infineon PMB6293	[-14; +142]	[-50;+7]
Agilent AGPM7863	[-4; +46]	[-16; +16]

Table 14.2 PA timing offset allowed range for different PA

15 Annex 2

NA

16 Annex 3

NA

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