Technical Note
32kHz RTC oscillator frequency jitter

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1 Document Mission/Scope

1.1 Mission

The present note specifies an observed 32 kHz RTC oscillator instabilty in frequency and in time (jittering).
The amplitude instabilty affects time stability on squared-wave CLK32K signal used internally.
The problem causes unacceptable errors during RTC calibration by SCCU for power saving's sleeping timers.
The problem does not affect sleeping period timings, nor issuing a calibration with C166 running code from internal RAM.
The problem was particularly evident on BP2_GLOBE2 and ARES/DbTEL boards, much less on BP2_GLOBE1 and BP2_evaboards.
The problem seems to have an hardware root cause.

1.2 Scope

The scope of this note regards HW and L1 power saving developers and integrators.

2 List of Acronyms

Abbreviation / Term	Explanation / Definition
SCCU	Standby Clock Control Unit
RTC	Real Time Clock
ob	Octal Bit
VCXO	Voltage Controlled Xtal (Cristal) Oscillator
DRX	Discontinuous RX (Reception)

3 Introduction

Baseband 32 kHz RTC oscillator is used to maintain real time clock date and time when the phone is turned off and for power saving purposes. Even if its nominal frequency is 32768 Hz, real quartz frequency may vary up to plus or less ten hertz, since its frequency is not absolute.

Since the quartz-oscillator is not tunable itself, and its frequency mainly depends from actual temperature and quartz age, a calibration process shall be periodically performed. Such a process is supported by hardware in the SCCU. Calibration is started setting bit SCCUSLPCTRL.REFEN by software. When calibration ends the same bit is reset by hardware.

Calibration of the RTC clock measures the time difference between 16 highly stable VCXO-referenced frames (i.e. about 73.846154 ms) and 16 * 151 unaccurate RTC clock cycles (at nominal frequency: 73.730469 ms) in 13 MHz clock cycle units (i.e. about 76.9231 ns units).
Since one VCXO-referenced frame length equates 60000 13 MHz clock cycles, the following "calibration expression" will give you the calibration value you will read from SCCUREFL.REFOUT register (nominal range is 0..7499) depending from actual RTC running frequency:

$$13000000 \cdot \left(\frac{60000 \cdot 16}{13000000} - \frac{151 \cdot 16}{f_{RTC}} \right) = SCCUREFL.REFOUT$$

Units are S.I. (Hz for frequency, s for time).

The calibration value SCCUREFL.REFOUT is then used to fine-tune the sleeping periods exactly to an integral number of frames, cascading a coarse slow-speed timer running at 32 kHz and a fine 26 MHz fast timer (affected by calibration value).

The calibration value shall be accurate to LSB, since 1 LSB error reflects in $\frac{76.9231ns}{73.846154ms} = 1{,}04167\text{ppm}$.

If an inaccurate calibration of RTC is performed, an error of 0.49 μs/LSB_{ECOREF} (about 1 ob) occurs on every CCCH radio block occurence on network normal paging period (DRX) 2, or 2 * 51 frames.

This error rises up to 2,2 μs/LSB_{ECOREF} (about 4.8 ob, more than half symbol bit) if network normal paging period is 9 (9 * 51 frames).

On PCCCH channels, where the paging period can potentially be up to 64 * 52 frames, or 15.36 s, the situation could be even worst.

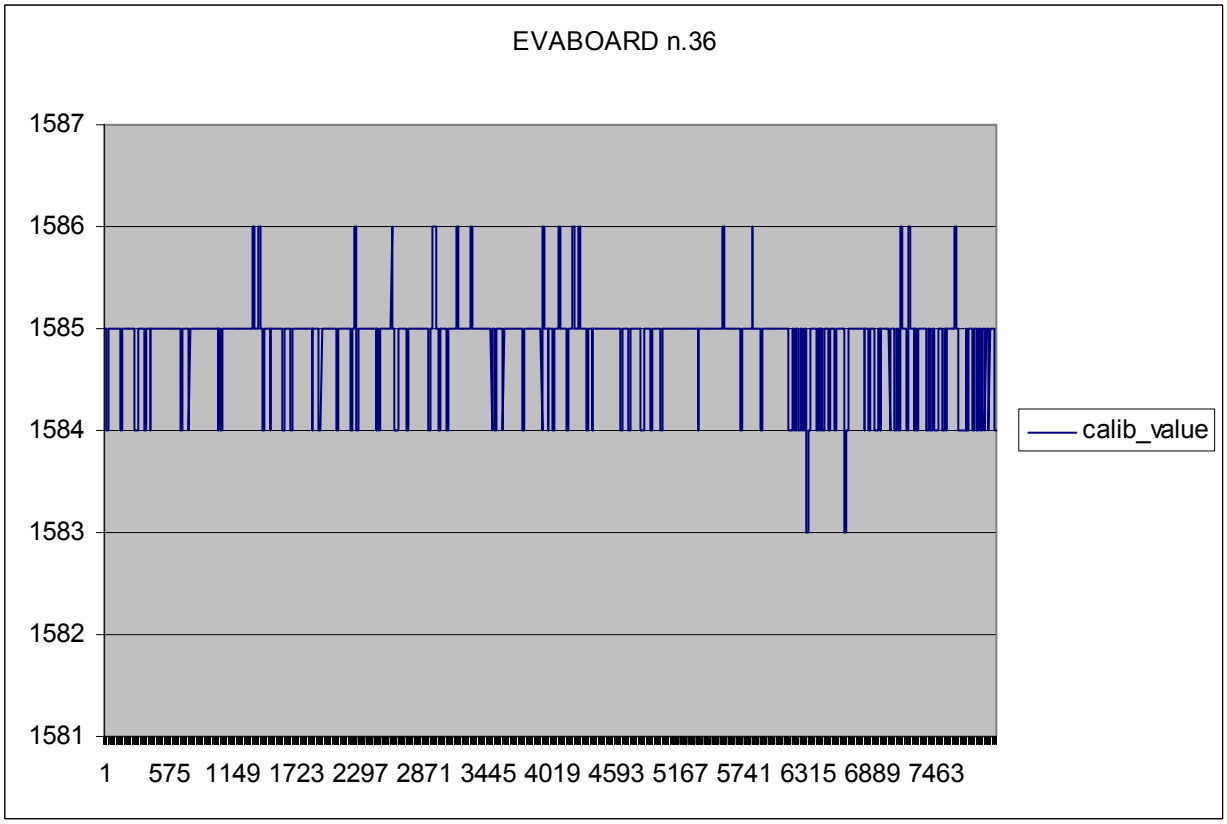


Figure 3.1 – EVABOARD calibration value (REFOUT) log

calib_value average	1584,8653
calib_value variance	0,1913183
average RTC frequency (Hz)	32770,768
Time Base delay to 151 * 16 RTC cycles (ms)	73,724241

Table 3.1 - EVABOARD calibration value (REFOUT) statistics and parameters

4 RTC frequency jitter

Calibration, that is to say RTC frequency, values reported on some EGOLD-lite based boards are seen highly repeatable (i.e. predictable from one calibration to next one), but on some other boards the calibration value is quite unpredictable.

This appears to be caused by a jitter on RTC clock signal during the calibration is running.

A case study classification was performed on modified 04.07 stack-only code:

1) on calibration trace values;
2) on digital CLK32K signal pad;
3) on analogue RTC oscillator;

Jitter of the RTC clock during the sleep phase does not appear to be a problem. In fact for proper fixed calibration values, sleeping phase proceed absolutely correct. This aws explained by the fact that the jitter amount is smaller when VCXO and C166 activity is stopped. Please refer to Para 6.

Original code was modified to enforce an RTC calibration after every normal paging, after at least 1000 frames were elapsed. Practically speaking, a calibration occurs about every 5 to 8 seconds, depending on DRX value selected.

In the following measures DRX was set to 2 to guarantee minimum timing offset errors on paging radio blocks, since system corrects time base approximately every half second.

4.1 Calibration trace values

A software-only verification is performed using LLT.

Calibration value is traced by activation of LLT group gsm_l1_general|6, type gsm_l1_sleep_status|2 only. This can be commanded with `AT+XL1SET="L6 2"` command.

Calibration values were filtered and extraceted with a text editor and imported into Excel file.

The result of calibration values on EVABOARD (id. n.36) are reported in Figure 3.1 and Table 3.1 reporting 8000 consecutive calib values:
The result of calibration values on GLOBE2 (id. n.141) are reported in Figure 4.1 and Table 4.1 reporting 8000 consecutive calib values:

It is immediately seen that the calib_value variance is very good on EVABOARD, while it is unacceptable on GLOBE2 board.

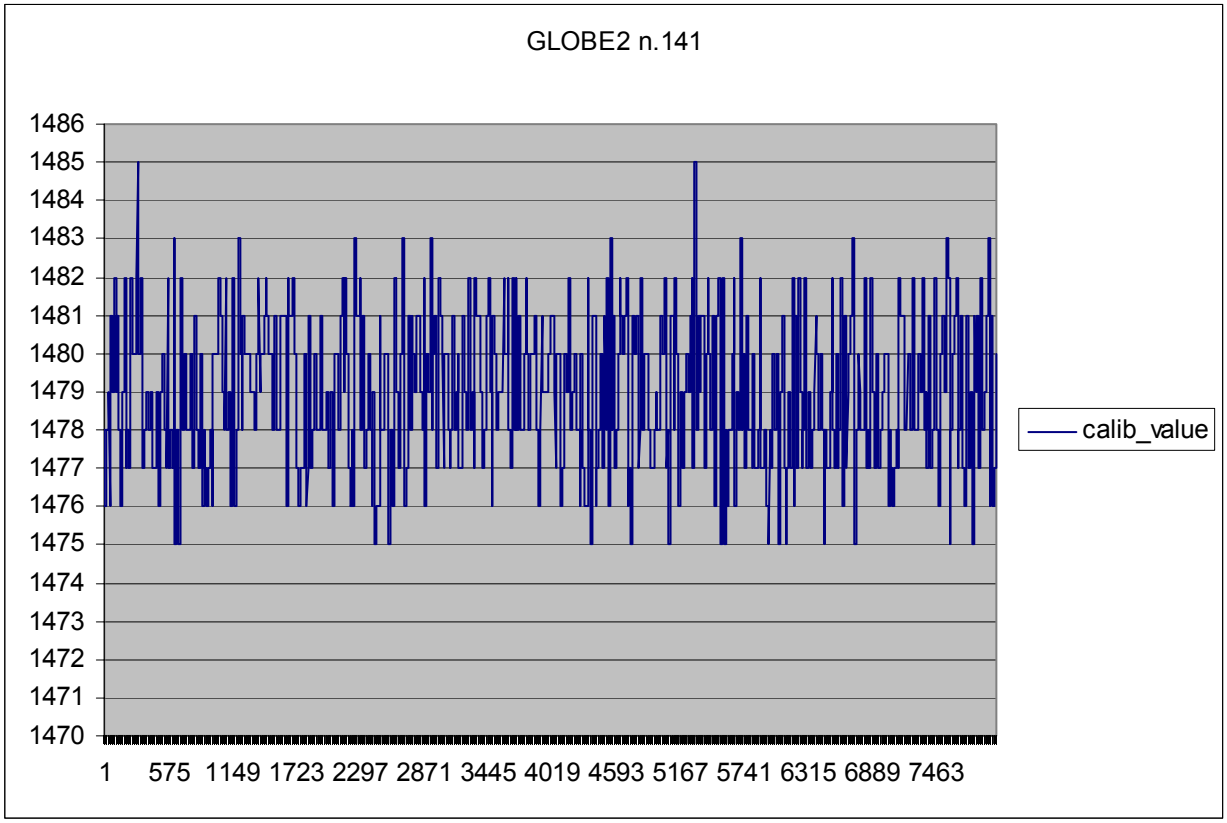


Figure 4.1 – GLOBE2 calibration value (REFOUT) log

calib_value average	1478,957114
calib_value variance	3,999536101
average RTC frequency (Hz)	32767,14709
Time Base delay to 151 * 16 RTC cycles (ms)	73,73238791

Table 4.1 – GLOBE2 calibration value (REFOUT) statistics and parameters

4.2 Digital CLK32K signal pad

For a hardware investigation, the squared RTC signal jitter over 151 * 16 clock cycles was measured in the following way.

The CLK32K signal is enabled setting in modified code bit 9 of MST_CLK_CTRL. Then the signal is can be monitored externally on following possible pins:

Ball coord	***Pin Name***	***Alt Function***	***GPIO***	***Actual usage***
M5	RFSTR1	Alt 2	GPIO_37	On GLOBE2 as IRDA/serial port 0 selector. On EVABOARD to SIM level shifter (not used)
N3	SSC1_MTSR	Alt 1	GPIO_54	On GLOBE2 as soft I2C clock to E-POWERlite On EVABOARD to SSC1 connector (not used)

Table 4.2 – CLK32K pad ball, pin and function mapping

Since software I2C bus driving the E-POWERlite cannot be rewired nor overridden easily, the CLK32K signal was enabled on ball M5, RFSTR1 pin, Alt function 2, for these tests.

A GPIO (GPIO_21, already used for driving red led, mapped on ball R3, pin name I2S1_RX), was used to generate a calibration gate signal. The GPIO signal goes high exactly when the hardware calibration process (immediately after setting SCCUSLPCTRL.REFEN). GPIO is resetted when SCCUSLPCTRL.REFEN is detected low (by polling, once per frame) indicating an end of the calibration process.
Hence GPIO calibration gate signal duration is a bit larger than real calibration period, up to 1 frame more (78.35 ms).

Note that, avoiding to use a modified code, it is possible to use also the monitor signal **tststate13m_0** that goes high about 210ns after the calibration started and goes low 210 ns after 151 * 16 RTC clock cycles elapsed. Such a signal can be extracted on proper pin MON2 using the AT extended command AT+XL1set="MON:2 032d".

To see on the scope the 32 kHz jitter during calibration period only, a pattern "smart" trigger was used.

Trigger was programmed to strobe on third negative edge of the 32 kHz clock occurring after calibration gate is active. The trigger was then delayed by the expected 16 * 151 = 2416 RTC clock cycles, allowing to zoom around the the 2416th falling edge of the clock, that is to say the last edge of the hardware calibration. A preventive average frequency measurement is done to know the period length.

Use Trigger/More, Sequence with following settings:

Sequence Stages

First, find:
Pattern 1 Entered
Then, trigger on:
Nth Edge 2
Reset on:
No Reset

With:

P1: 1 XHXX 4 Ext X
P2: 1 XXXX 4 Ext X
E1: 1 XXXX 4 Ext X
E1: 1 ↑XXX 4 Ext X
N = 3
Timeout = *do not care*

Then time base was stretched up in non-interleaved acquisition (Real-Time) mode. Use Waveform/Acquire/Realtime menù to use fastest timebase without undesired interleaving. Remember to set also an holdoff greater than 78.35 ms (e.g. 80 ms) to avoid false strobes.

If using monitor signal **tststate13m_0** a simpler Pattern trigger can be used, set as follows:

Pattern = 1 ↑HXX 4 Ext X

taking into account that the contribution to jitter of the first RTC clock cycle is neglible and looking for jitter of remaining 151 * 16 – 1 = 2415 RTC clock cycles.

Under either of these conditions we turned on "persistence mode" to record falling edge jittering.

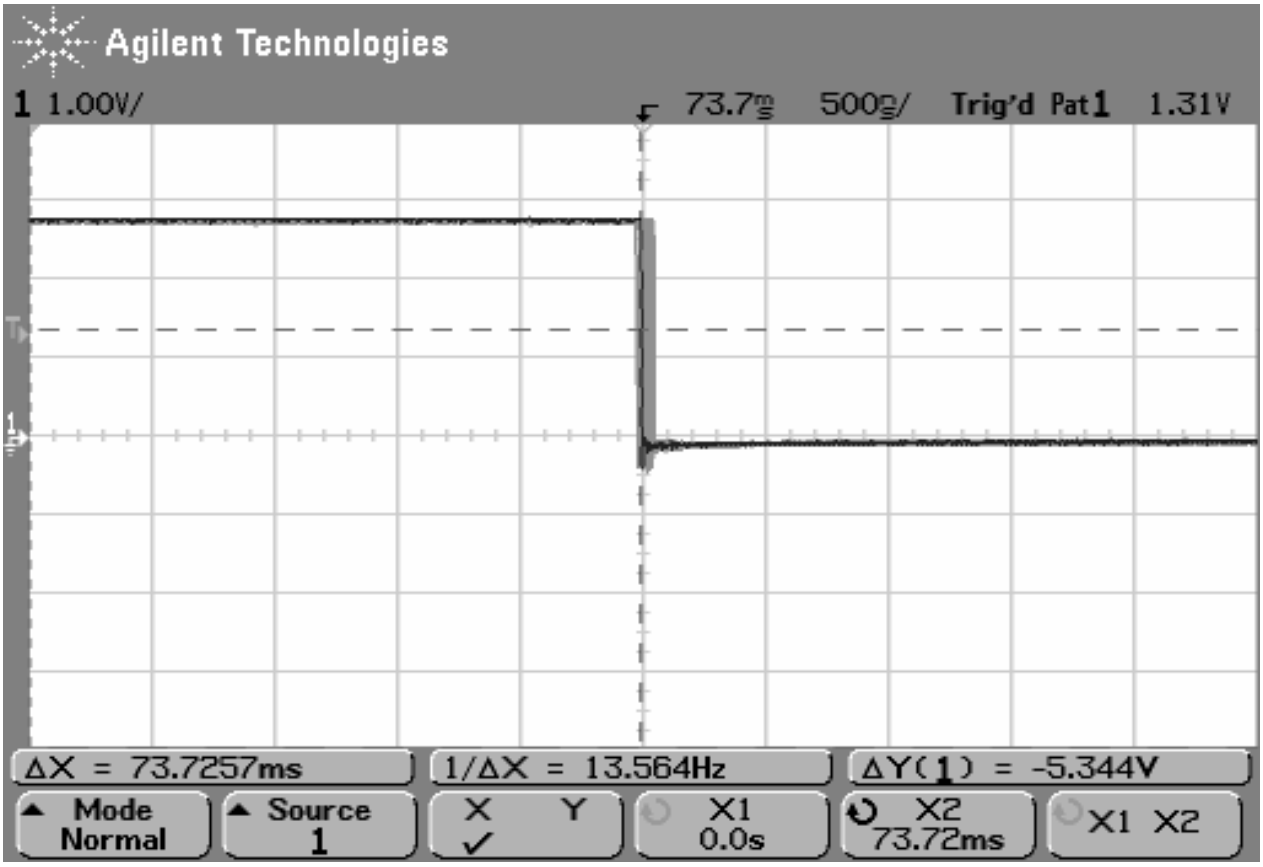


Figure 4.2 – EVABOARD CLK32K signal jitter at the end of the calibration period.

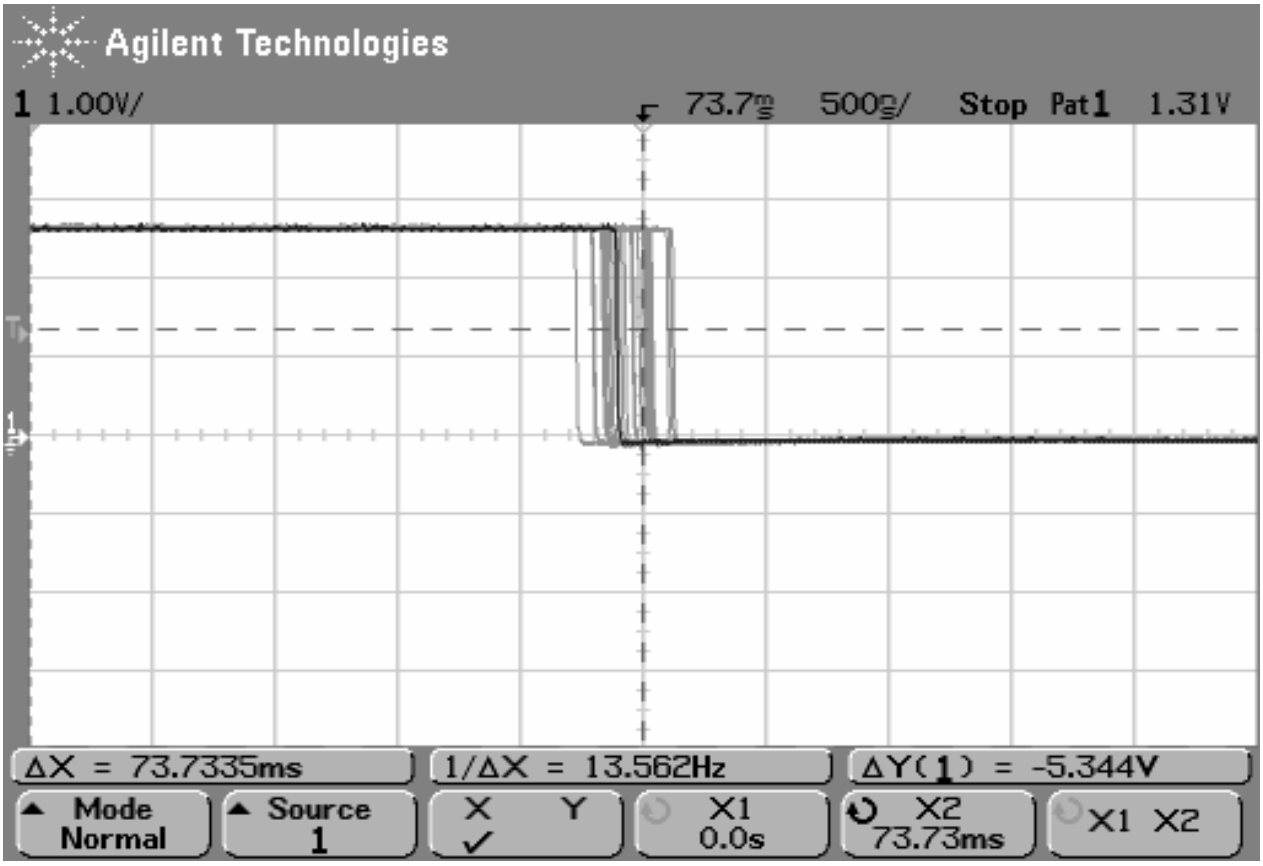


Figure 4.3 – GLOBE2 CLK32K signal jitter at the end of the calibration period (original artwork).

Results were reported in Figure 4.2and Figure 4.3.

It is readily seen that GLOBE2 boards have extremely high jitter on CLK32K at the end of the calibration period, compared to EVABOARD.

So an hardware rework was done: the quartz and relevant capacitors were desoldered, then routes for F32K (RTC oscillator output, ball A9) and OSC32K (RTC oscillator input, ball A8) were cutted to 2 mm lenght away from the E-GOLDlite chip ball and components were flying-mounted again to reduce possible passive couplings. Moreover a micro shield was installed around the cristal oscillator flying circuitry to enhance stability. The scope result is greatly improved and can be seen in Figure 4.4.

A possible reason of the problem so fixed could be found in a long route to external high impedance buffer connected from F32K output used to feed 32kHz to TEA5767HN FM Radio circuitry. Cutting traces to 2 mm the long route to the 32 kHz buffer was isolated, hence mainly reducing the jitter.

You should also note that since such a measurement observes for 16 * 151 = 2416 32 kHz cycles it should be also possible to monitor the rtc_clk_32k line through MON1 or MON2 lines programming MON_CR1 or MON_CR2 registers with 0x0318.
In this case, since MON1/MON2 reports the half of real clock signal we will observe the 1208th falling edge transition but jitter will be identical at the end of the calibration period. You can use, for example, the on-line AT command AT+XL1SET="mon:1 0318" to easily watch the halved RTC 16kHz signal on MON1 pin.

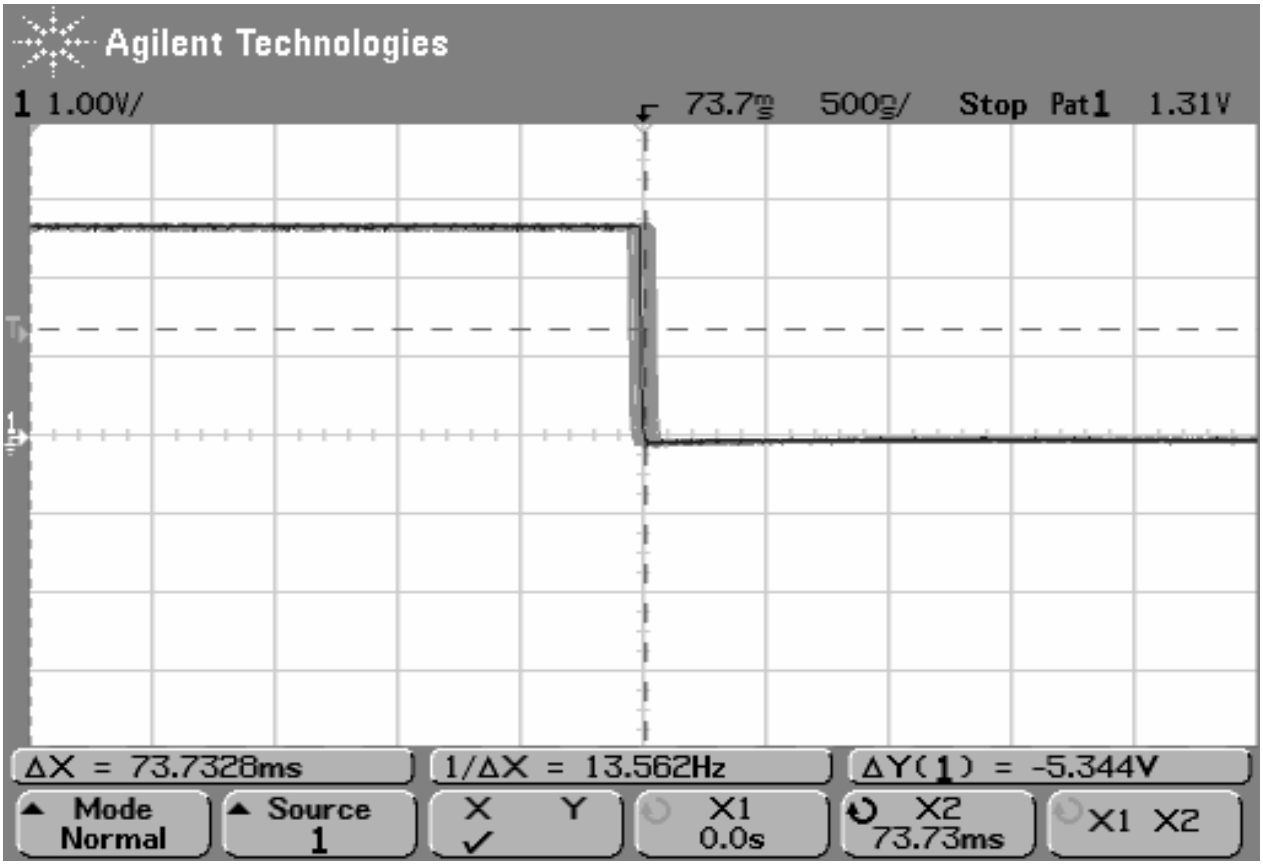


Figure 4.4 – GLOBE2 CLK32K signal jitter at the end of the calibration period (shielded oscillator).

4.3 Measures on analogue RTC oscillator

A direct analog measure is also possible on F32K (osc output) and (eventually) on OSC32K (osc input). Such measure is very critical, since high impedance of the oscillator circuit can be affected by probe input impedance, expecially by the reactive (i.e. capacitive) component.

Measurement can be performed using an active probe. Alternatively, a probe direct measure shall take into account the probe capacitance of 15 pF that requires to substitute the 18 pF with only 3 pF with probe always connected. A capacitor in series to probe allows to decouple 10 Mohm resistive component, too.

Analog measure was made on the GLOBE2. In Figure 4.5 you can find an extract of the RTC oscillator layout:

It was seen that sub-armonic components are superimposed onto the 32 kHz fundamental, thus giving something like odd and even cycle average amplitude values lower and higher. This can reflect from amplitude to time jitter, since a given threshold is used.

On top trace you can see VCXO_en (In Figure 4.6 showing that the clock master is still running slowly when rising up, in Figure 4.7 when VCXO is running at full speed after 1 frame of WAIT time for VCXO to run-in), while in bottom trace the AC coupled F32K is reported:

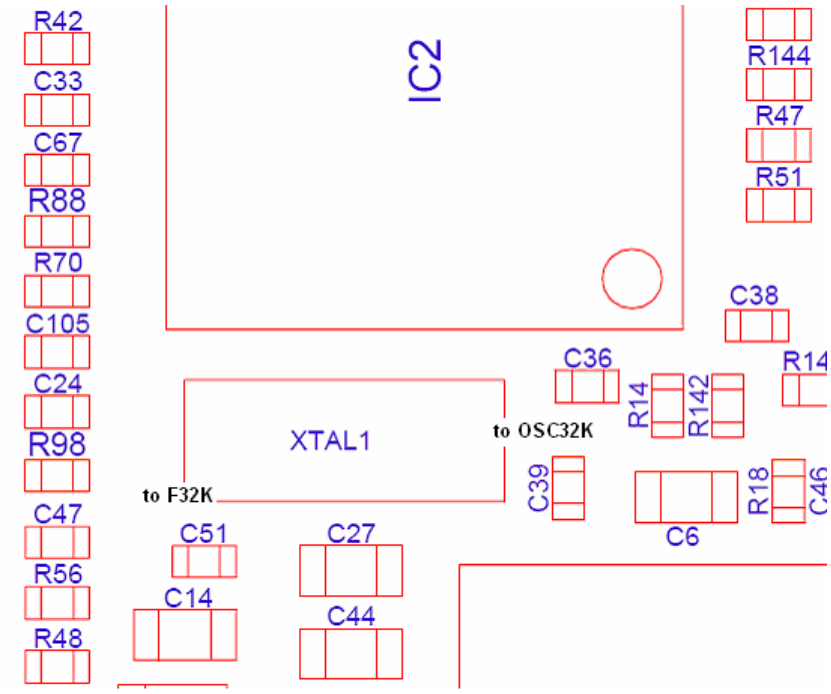


Figure 4.5 – GLOBE2 RTC oscillator layout

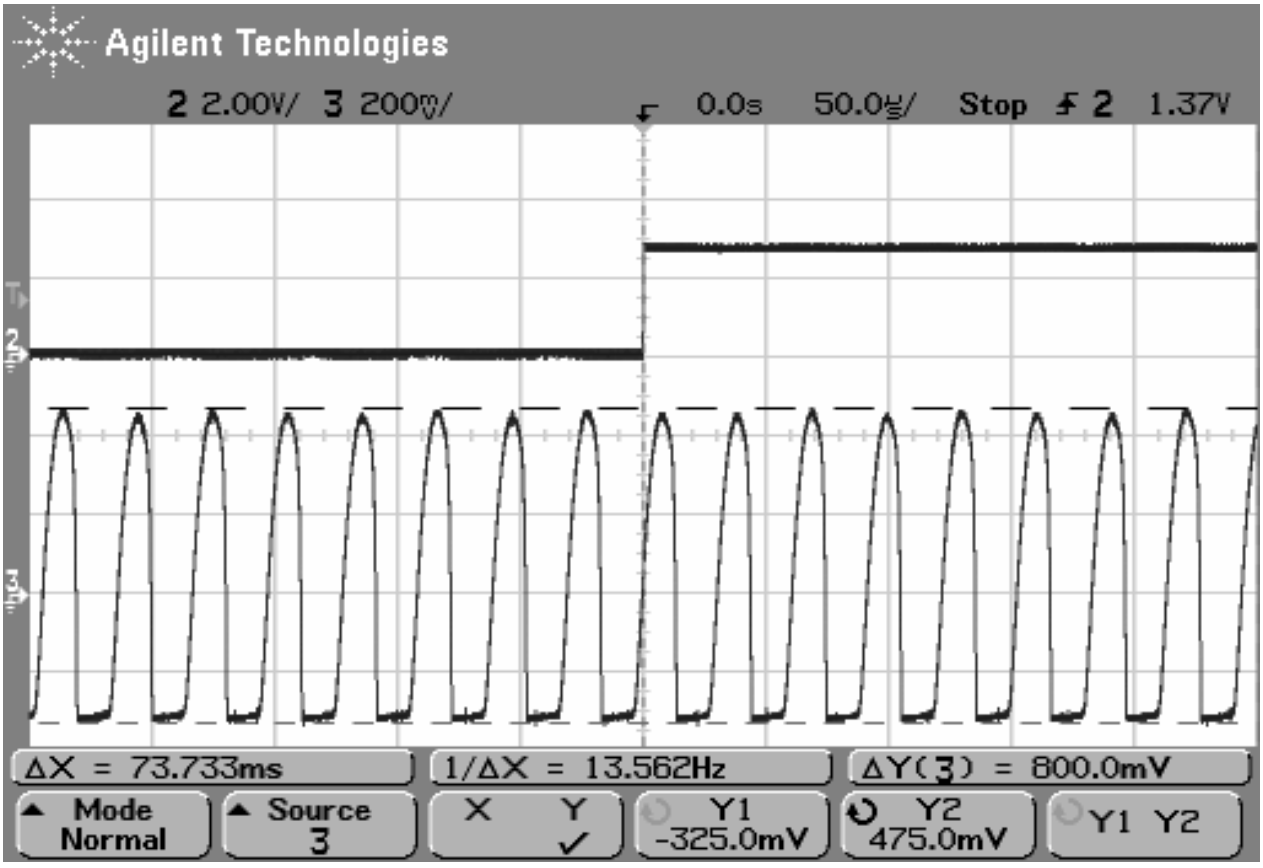


Figure 4.6 – GLOBE2: F23K swinging when VCXO is stopped

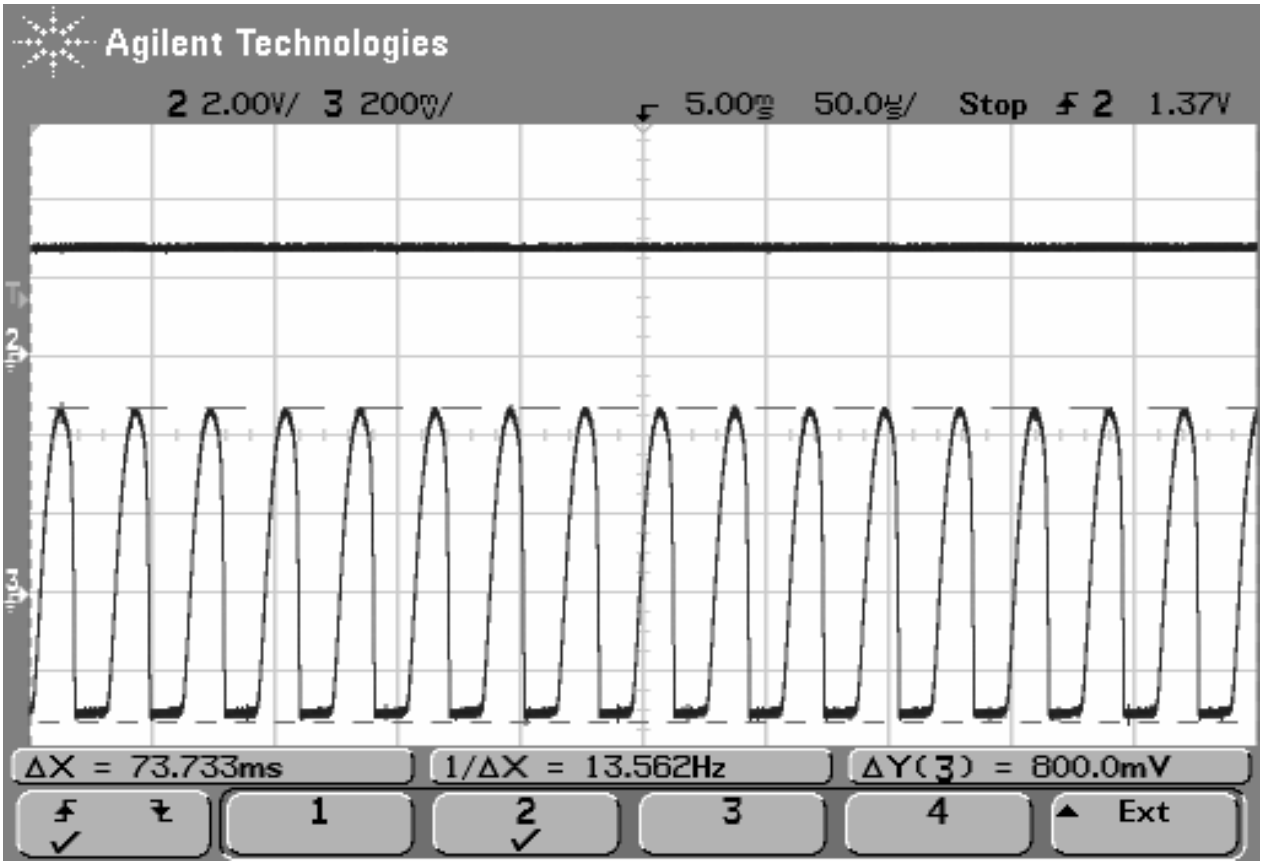


Figure 4.7 – GLOBE2: F23K swinging when VCXO is running (after 5 ms the VCXO_en ridsing edge).

The analog waveform shows an under-biasing and a very slight amplitude modulation.

In any case, for time jitter, it is better to look CLK32K (or MON1/2 rtc_clk_32k halved frequency monitor signal).

Using very slow timebase, instead, we can observe that the amplitude envelope is clearly present during the VCXO enabled periods (Figure 4.9).

4.3.1 Oscillator I/O modeling

Possible noise sensitivity can be caused by high impedance / high gain of the onchip oscillator. Hence an impedance modeling of the input/output on-chip oscillator was made.

DC point measurement for bias and low signal level input and output impedeance was made.

DC bias was detected with the help of a couple of 1.5 uF low loss caps in input and in output. After a while the bias voltages are stable, regardless of the input/output impedance if measure is performed quickly with an high impedance multimeter.

Ball	Pin name	Signal	Average bias level
A8	OSC32K	Input of oscillator	225 mV
A9	F32K	Output of oscillator	281 mV

Table 4.3 –Average biasing of 32kHz oscillator

VRTC power supply voltage: 2.088V.

Loading pins with multimeter impedance (normal = 10 MΩ / low impedance = 415 kΩ) and measuring input and ouput voltage vs ground and supply we extimated the pin impedances as follows:

Input impedance: ≈14 MΩ
Output impedance: ≈25 kΩ (17 kΩ sink, 32 kΩ source). Source/sink asymetry detected, may be due to a common source output stage.

With nominal oscillator circuit, but input capacitance of 180+15 pF, AC measure reports approximately that oscillator gain is 418 mV / 28 mV = 15 at 32 kHz. The oscillator amplifier makes a 180° phase shift at 32 kHz. Amplification reduces with increasing input signal level, due to saturation effects.

Schmitt trigger thresholds on oscillator output results to be 68.8 mV (Low logic) and 325 mV (High logic) (Figure 4.8).

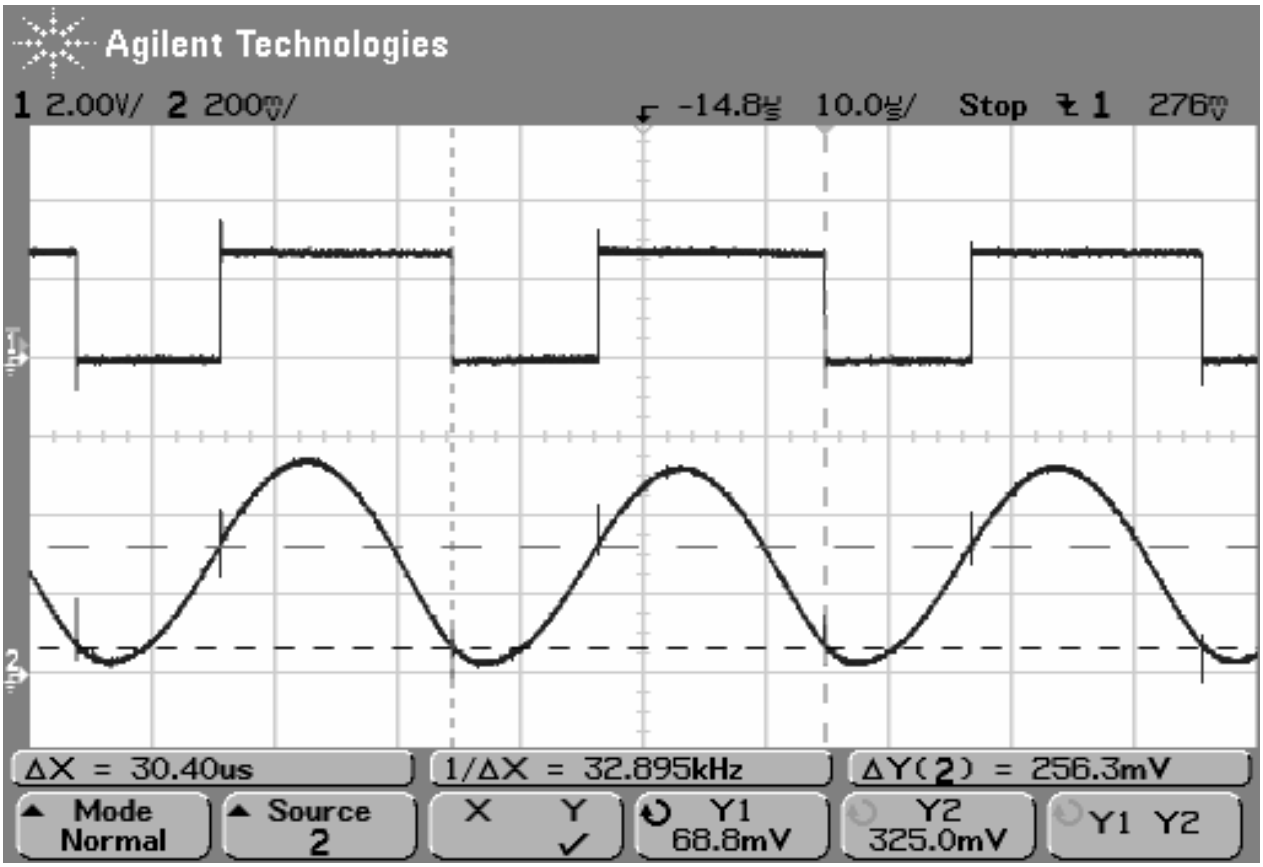


Figure 4.8

4.4 DbTEL / ARES board

The 32kHz jitter can be also clearly seen on ARES Proto-2 board during calibration. There is no apparently long route, like in the GLOBE2 board, but only a slight coupling with most of address and data bus. Here we suspect total distributed unshielded capacitance causes the jitter problem

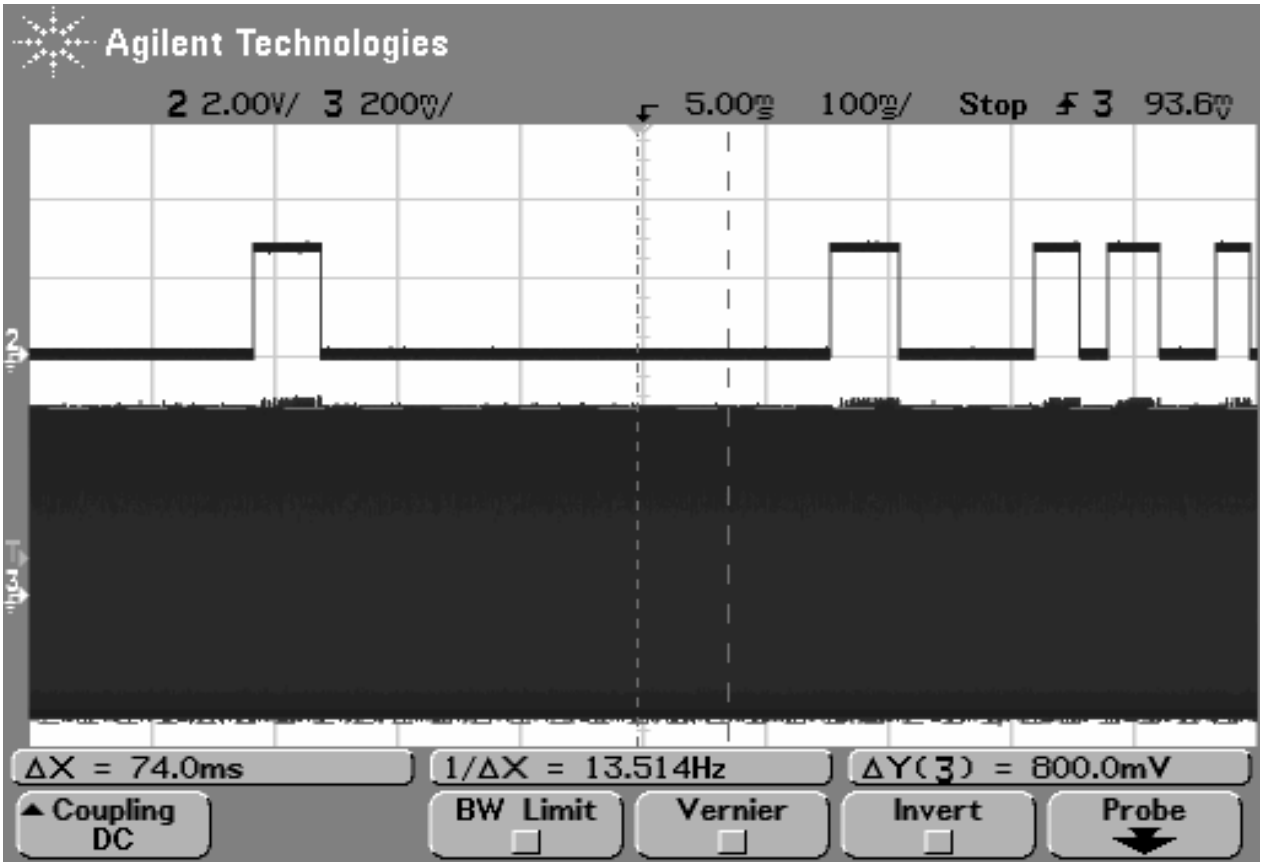


Figure 4.9 – GLOBE2: Amplitude envelope of CLK32K during VCXO running periods.

5 Jitter during sleeping periods

While the sleep mode is running jitter is also present but its amount is absolutely neglible respect to the slept period.

To evaluate jitter on sleeping period, measure it indirectly looking simply to VCXO_en signal, since it is synchronous on 32 kHz rising edges. Then, after WAIT period elapsed, measured in 32 kHz cycles, the stabilized VCXO clock is used to finely wait remaining time to real world frame alignment using previous calibration value.

We can measure the jitter, triggering on falling edge of VCXO_en, placing proper delay (see below) and zooming in after time delayed. No need for holdoff is required and display persistence shall be used. Multiple sleeping period will be normally discarded since normally it is impossible to equate the number of RTC cycles obtained in single slept period.

Preferred time delays will be:

1) maximum allowed sleeping time of 400 frames, when paging period 8 or 9 is selected: this period has to be reduced by 1 frame (GLOBE1, GLOBE2, ARES) for VCXO prewakeup, that is to say 399 slept frames. Hence VCXO_en will stay low for 151 * 399 – 6 = 60243 RTC clock cycles. This usually represents the most critical situation.
2) Depending from selected paging period (DRX) when 7 or less as reported in Table 5.1.

Paging Period	Sleeping time in frames	VCXO_en low in 32 kHz cyles
2	2*51-5=97	(97-1)*151-6=14490
3	3*51-5=148	(148-1)*151-6=22191
4	4*51-5=199	(199-1)*151-6=29892
5	5*51-5=250	(250-1)*151-6=37593
6	6*51-5=301	(301-1)*151-6=45294
7	7*51-5=352	(352-1)*151-6=52995

Table 5.1 – Paging Period and slept frames

In Figure 5.1 is shown the jitter over maximum allowed slept period measued on GLOBE2 board n.141 with shielded oscillator. Max jitter is +/- 460 ns, or +/- 1 octal bit, that is, fortunately, absolutely neglible. Used calibration value was avaraged over several frames to get the best base synchronisation.

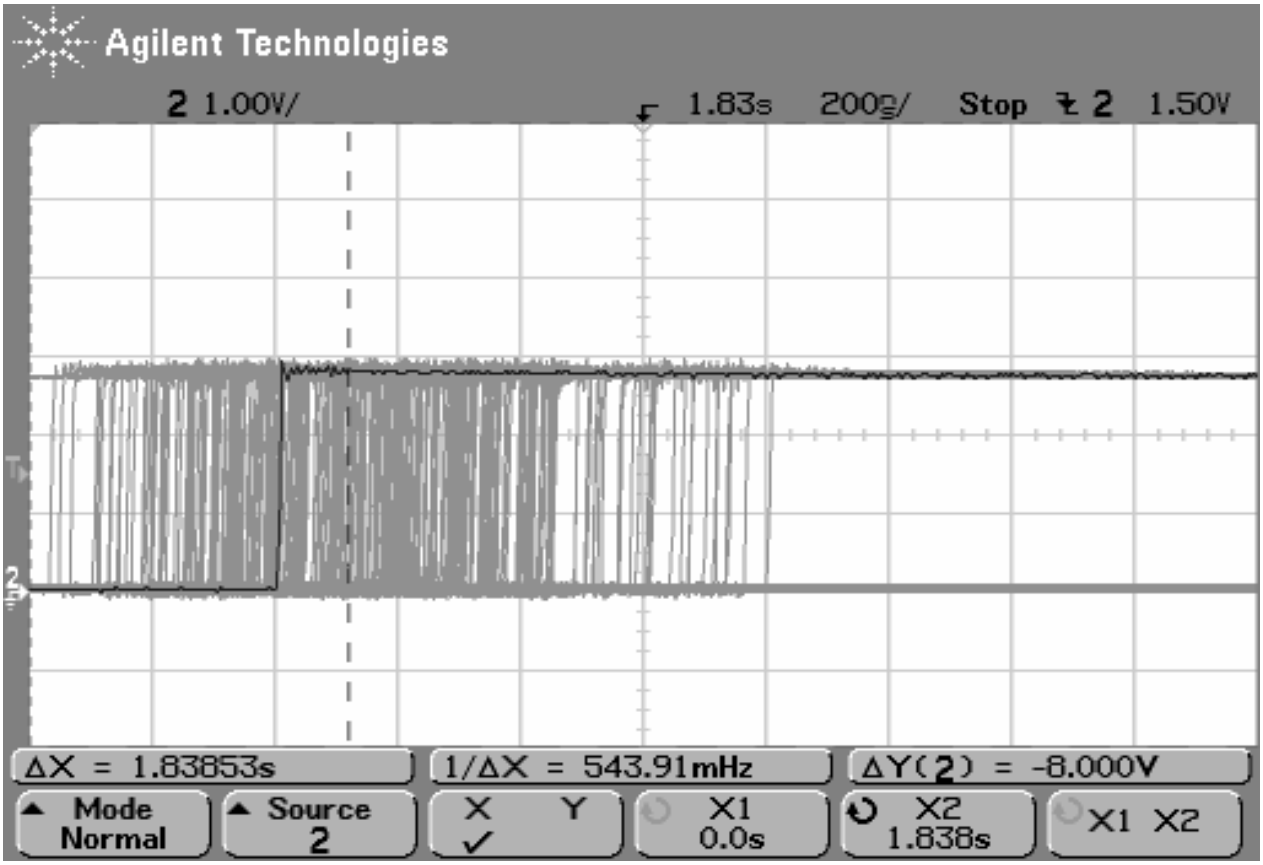


Figure 5.1 – Sleeping mode jitter on VCXO_en signal low on 400 slept frames (60243 RTC clock cycles)

The jitter decreases in a quite linear way with faster paging periods down to +/- 100 ns.

On ARES/DbTEL boards the jitter while in sleep mode were comparable to the reworked GLOBE2 n.141. Jitter is about +/- 100ns with 14490 RTC clock cycles sleep time and about 400ns with 52995 or more RTC clock cycles sleep. Please refer to Figure 5.2, Figure 5.3 and Figure 5.4 for further details.

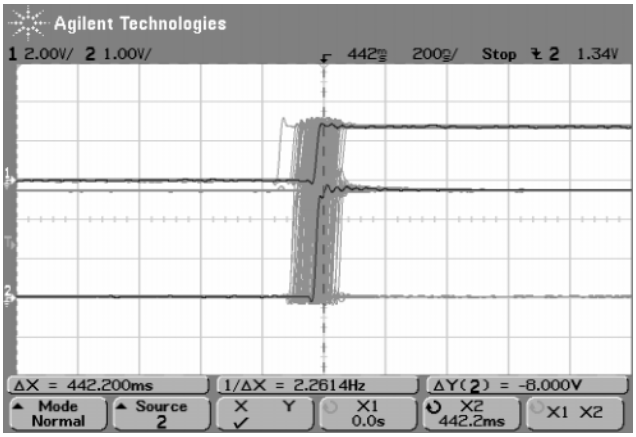


Figure 5.2 – ARES board sleep mode jitter with DRX=2 (14490 RTC clock cycles)

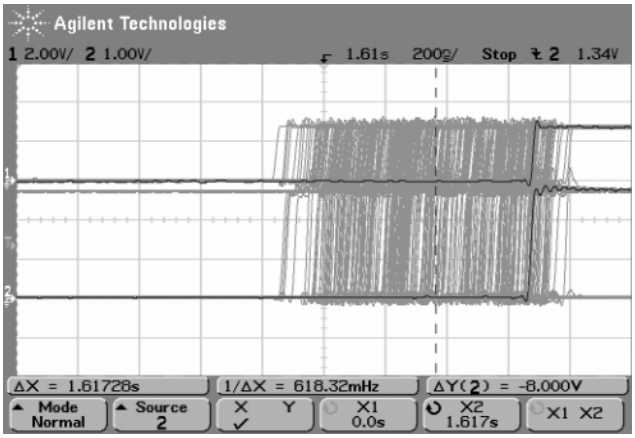


Figure 5.3 – ARES board sleep mode jitter with DRX=7 (52995 RTC clock cycles)

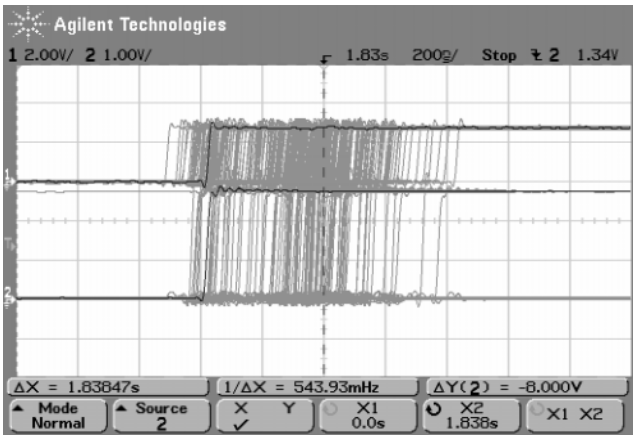


Figure 5.4 – ARES board sleep mode jitter with max 400 slept frames (60243 RTC clock cycles)

6 Calibration running from internal RAM

Starting from n7_bp2_04.21_fabrizioba/LATEST version the calibration approach was completely changed.

The calibration is called just before activating the sleep phase if more than 16 frames are available (one calibration duration). This allows to activate a calibration from internal RAM without accessing external RAM / Flash just immediately before entering sleep phase, thus making RTC calibration free from radiated noise and even much more accurate.

We also noted only on ARES/DbTEL board that even if the calibration procedure is executing from internal RAM, the RTC jitter significantly reduces if we program C166 prescaler to its maximum division factor, thus reducing C166 clock from 26 MHz to 203125 Hz. This is mainly related to chip internal radiation, but such a problem was not detected on GLOBE2 board. This behaviour is under further Investigation.

In any case an high C166 prescaler value allows power consumption to be reduced, and is always recommended with code running from internal RAM.

If the Flash shadow procedure copy is called, instead of the internal RAM copy, RTC jitter now can be seen very clearly. C166 clock shall be left at 26 MHz speed and cannot be switched down to 203125 Hz, else malfunctions occurrs on pseudostatic RAM accesses. Such a situation is very similar to the original calibration approach, that leaves running C166 on external address/data bus, with very similar results.

So calibration run from IRAM seems to be the final solution for 32kHz jitter. Now jitter is about +/- 10 to +/- 20 ns over one calibration period, thus guaranteeing always valid one-shot calibration results.

All the results of RTC clock jitter measurement during calibration with CPU looping idle in internal RAM or external Flash over ten minutes can be found in Table 6.1. Pattern trigger windowi on monitor signal **tststate13m_0** is used.

Trace 1 and trace 2 were connected to MON1 and MON2 programmed with AT+XL1SET="mon:1 0426" (RFSTR1 pad = CLK32K) and AT+XL1SET="mon:2 032D" (tststate13m_0)

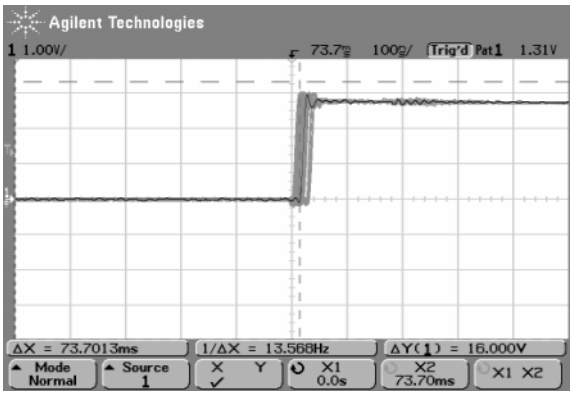
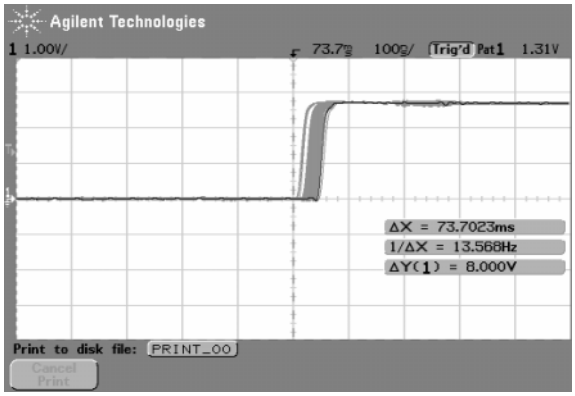
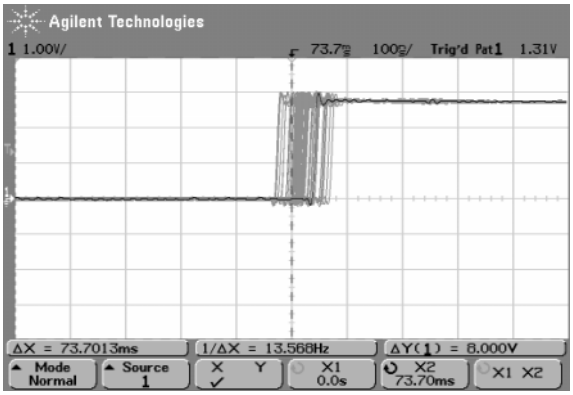
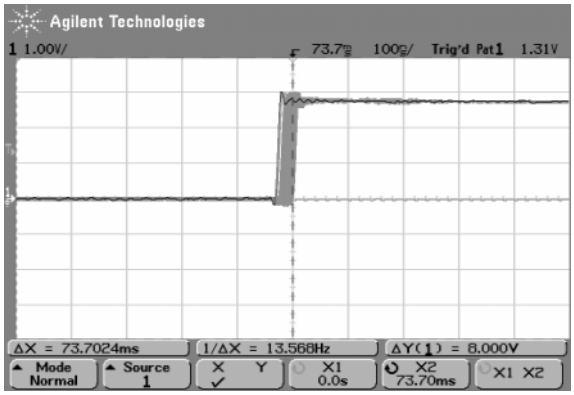
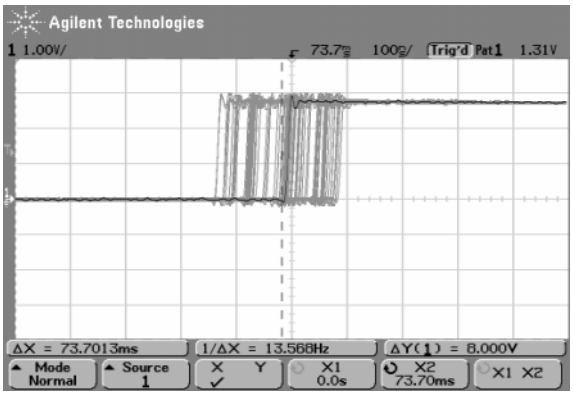
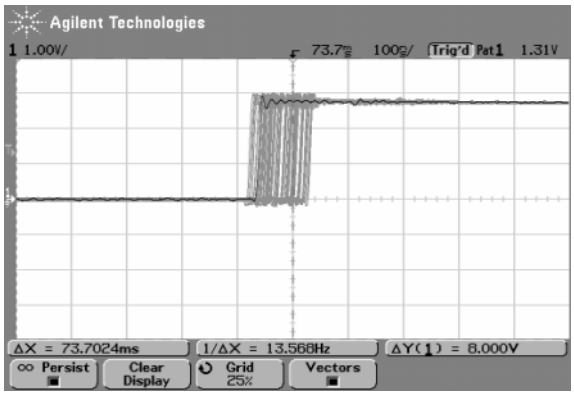
	ARES/DbTEL Proto2 board	BP2_GLOBE2 board n.141 (with osc. patch)
203 kHz IRAM code		
26 MHz IRAM code		
26 MHz Flash code		

Figure 6.1

Table 6.1 – Jitter measurement for RTC calibration and CPU waiting idle in internal RAM

7 Conclusion

The EGOLD-lite presents high time jitter instability caused by excessive oscillator sensitivity to adjacent signals. Some of this jitter can be reduced in come cases with accurate PCB design, but chip case internal coupling may be still present. Analog amplitude envelope is also present that affects the above time jitter.

Time jitter suppression is required expecially during RTC calibration to avoid page loss with high normal paging period values (e.g. 9).

Experienced EGOLD+ based existing project does not ever put in evidence such a problem.

Hardware and software solution can be applied to improve jitter rejection. Accurate RTC shielded design has to be done and an RTC calibration can be performed while CPU is looping idle into internal RAM with slow clock.

Pictures of hardware modified GLOBE2 (E-GOLDlite based) and MP1UE (SGOLD based) boards are reported in Annex 1. Red circles indicates the rework for RTC oscillator flying mounted.

The new calibration approach of running 32kHz XTAL calibration from IRAM shall be mandatory on all future hardware platforms to guarantee best time accuracy performances nd to avoid the risk of paging loss while in power saving. It could be extremely harmful removing the define IRAM_32K_CALIBRATION. The define USE_TOI_FOR_32K_CALIBRATION is highly suggested, even if not mandatory, to reduce explicit calibration at minimum, hence improving the power saving.
No behaviour check with the old calibration approach will be performed anymore.

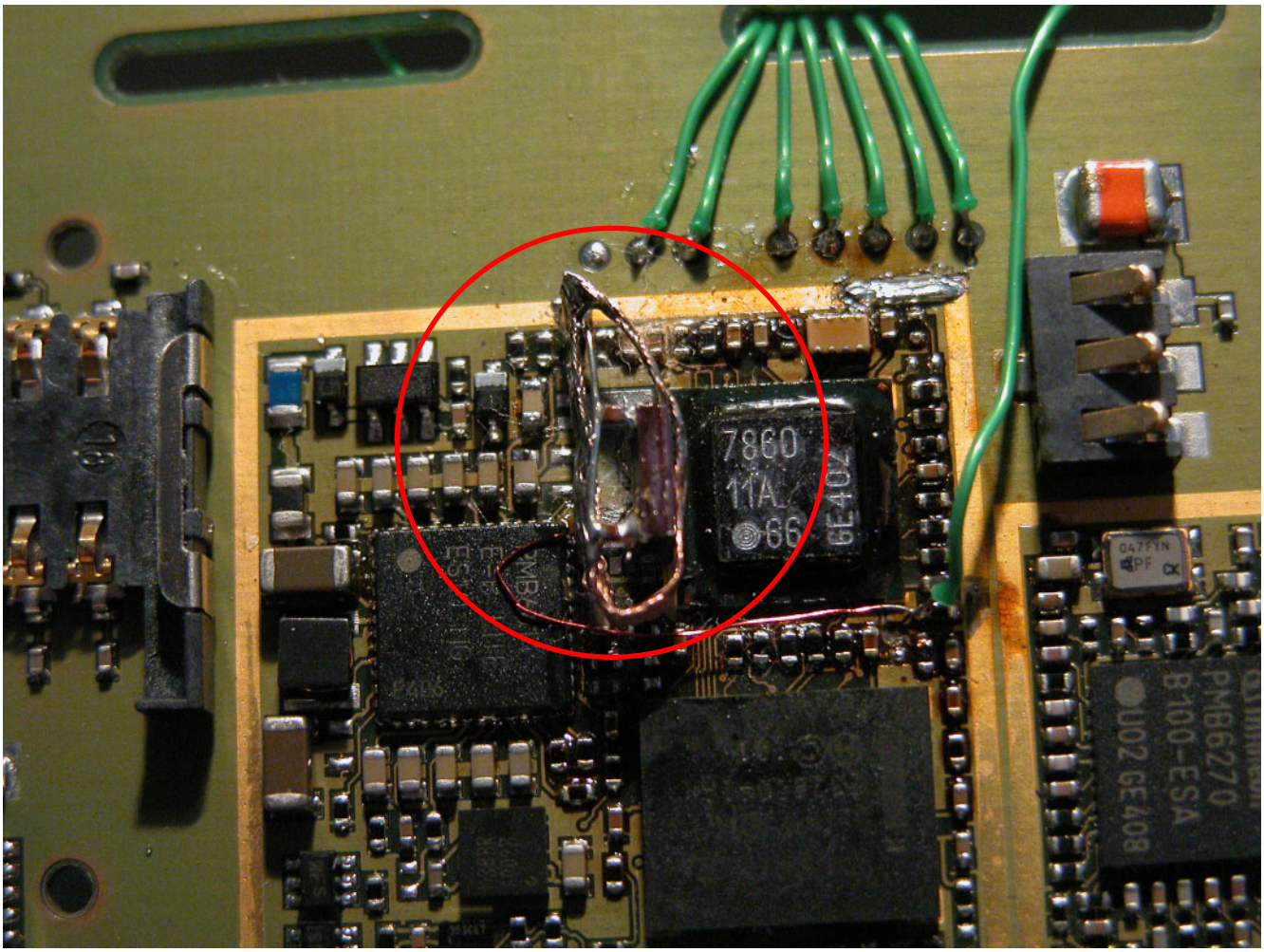
Document change report

	Change Reference		Record of changes made to previous released version	
Rev	**Date**	**CR**	**Section**	**Comment**
1.0	N/A	N/A	N/A	First issue
2.0	29/07/2004	N/A	4.3.1 Oscillator I/O modeling and 6 Calibration running from internal RAM.	New sections added. Document was reformatted.
2.1	18/01/2006	N/A	7. Conclusions	It was put in evidence the impact on all future hardware platforms.

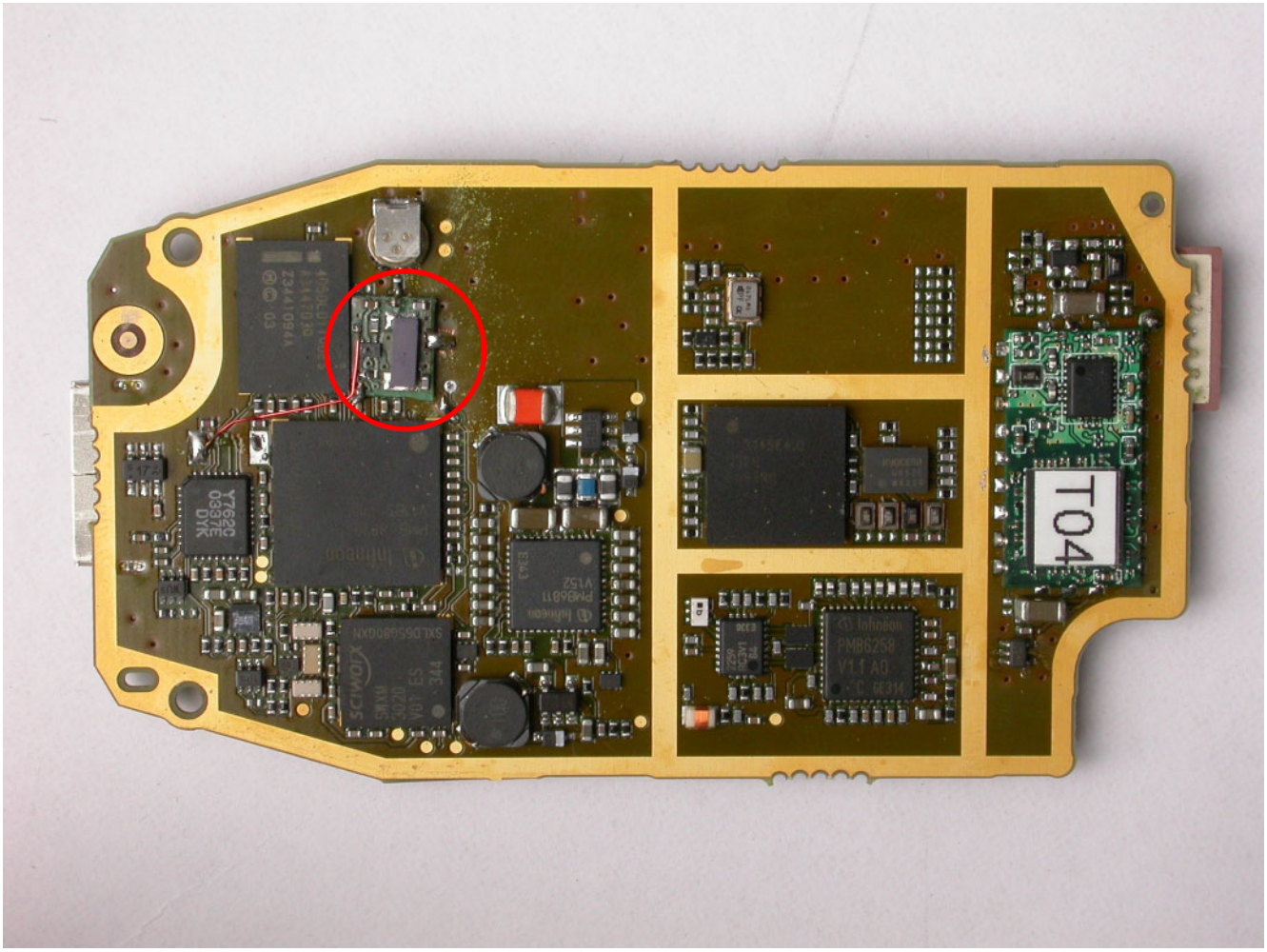
8 Approval

Revision	Approver(s)	Date	Source/signature
1.0	Stefano Godeas	09/07/2004	Document stored on server
2.0	Stefano Godeas	29/07/2004	Document stored on server
2.1	Stefano Godeas	18/01/2006	Document stored on server

Annex 1 – RTC oscillator patches



GLOBE2 n.141 – Shielded RTC oscillator patch



MP1UE – SGOLD PMB 8870-based mobile RTC patch (courtesy of Uwe Kliemann - COMNEON)